

KIUE0

Schematics Document

Mobile Penryn PGA with Intel
Cantiga_GM45+ICH9-M core logic

REV:1.0

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Compal confidential

Model Name : KIUE0
File Name : LA-5191P

TP Lock,HDD,Battery Charging,Power LED on MB
CAPS ,NUM Lock,BT,Wlan,NOVO,Power LED on Sub-Board

Mobile Penryn

uPGA-478 CPU

page 4, 5, 6

Clock Gen.

SLG8SP556VTR
ICS9LPRS387AKLFT

page 16

H_A#(3..35) FSB
H_D#(0..63) 667/800/1066MHz

Intel Cantiga GMCH

GM45

uFCBGA 1329

page 7, 8, 9, 10, 11, 12, 13

DDR3-800(1.5V)
DDR3-1067(1.5V)

DDR3-SO-DIMM X2

BANK 0, 1, 2, 3

page 14, 15

Dual Channel

UP TO 8G

DMI *4

C-Link

Intel ICH9-M

mBGA-676

page 19, 20, 21, 22

USB
5V 480MHz
PCIe 1x
1.5V 2.5GHz(250MB/s)
SATA port 1,5
5V 1.5GHz(150MB/s)

USB *6
5V 480MHz

USB Right
USB port 0
page 28

Int. Camera
USB port 2
page 17

BT conn
USB port 6
page 28

CardReader
USB port 7
page 25

FP conn
USB port 9
page 33

USB Conn
USB port 11
page 28

SATA port 0
5V 1.5GHz(150MB/s)

SATA HDD0
page 23

SATA port 4
5V 1.5GHz(150MB/s)

eSATA
page 23

USB port 4
5V 480MHz

USB Left
USB port 4
page 23

HD Audio 3.3V/24.576MHz/48MHz

Audio Codec

ALC272-GR

page 26

LPC BUS

EC

ENE KB926D3

page 31

Int.KBD
page 32

Touch Pad
page 32

SPI BUS

SPI ROM
page 30

G-SENSOR
page 28

Int MIC Conn

HP Conn

page 27

AMP-TPA6017
page 27

2-CH SPK
1.5W X 2

Sub-Board List

Finger Printer/B

Switch/B

Power/B

KB Light/B

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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5V	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+GPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for NB	ON	OFF	OFF	OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	CRT	LAN	Finger printer	BLUE TOOTH	3G SIM slot	Mini card
description	(Q)	(C)	(F)	(B)	(3)	(D2)
explain						
BTO						

External PCI Devices

EC SM Bus1 address

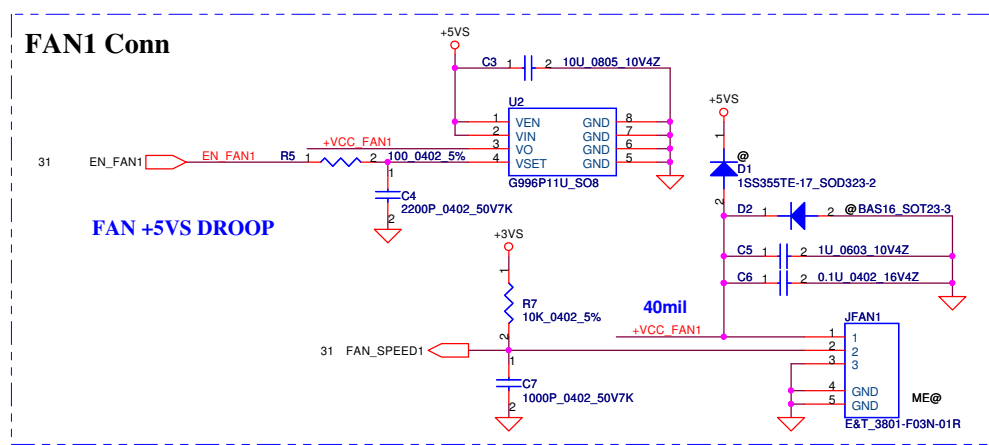
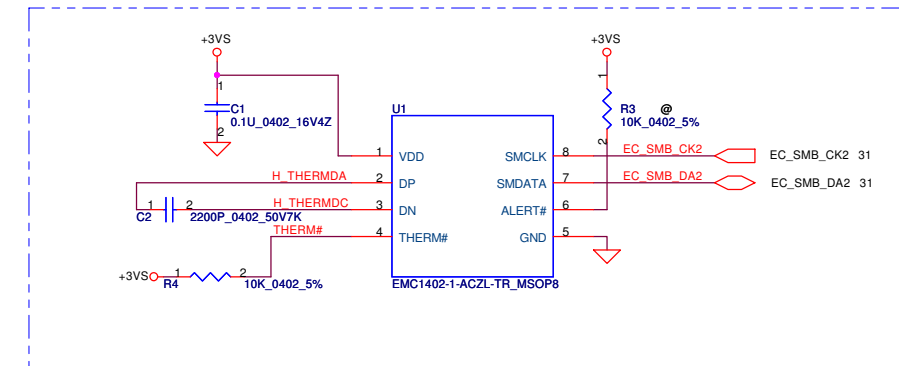
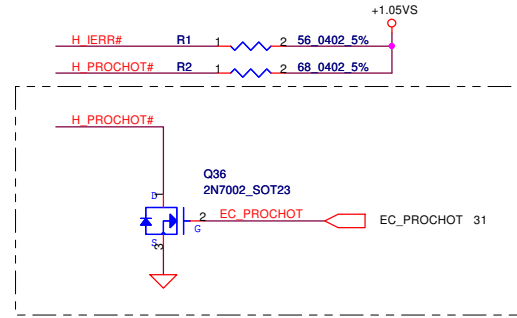
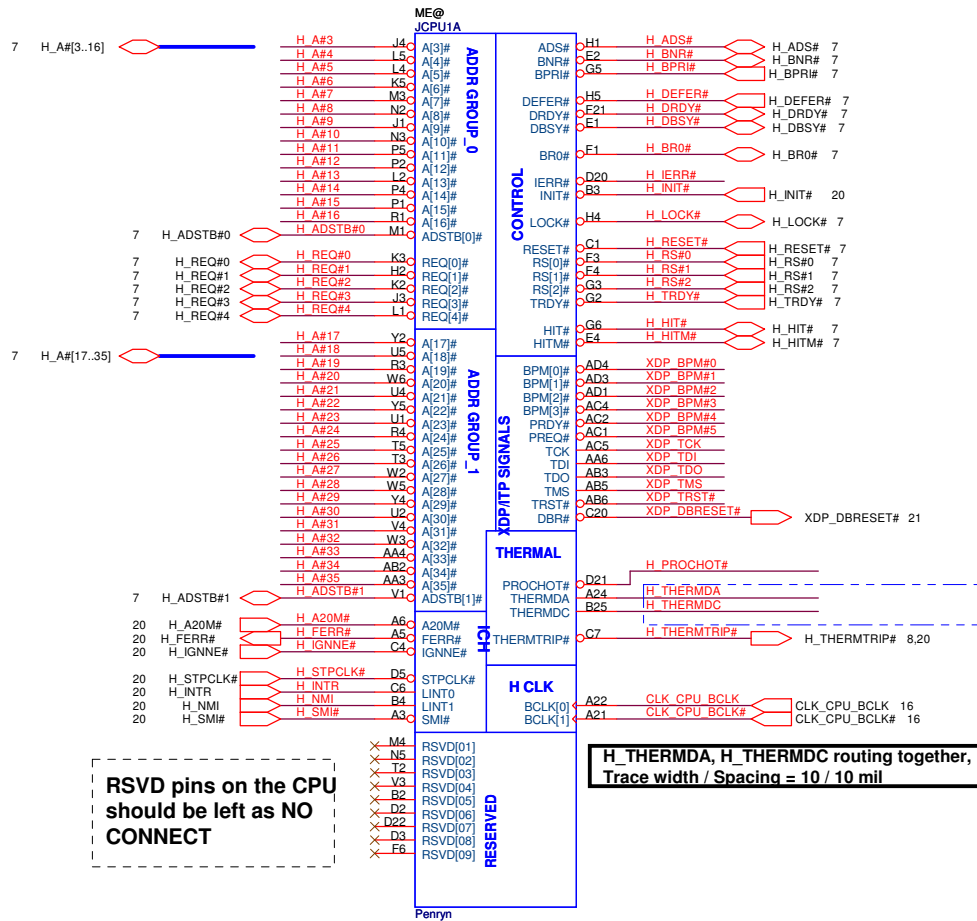
EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VALW	EC KB926 D3		+3VALW	EC KB926 D3	
+3VALW	Smart Battery			CPU THM Sen	
			+3VALW	SMSC SMC1402	

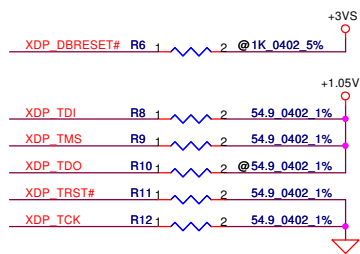
ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
	Clock Generator (SLG8SP556V)	
+3VS	DDR DIMM0	
+3VS	DDR DIMM1	
+3VS	Express	

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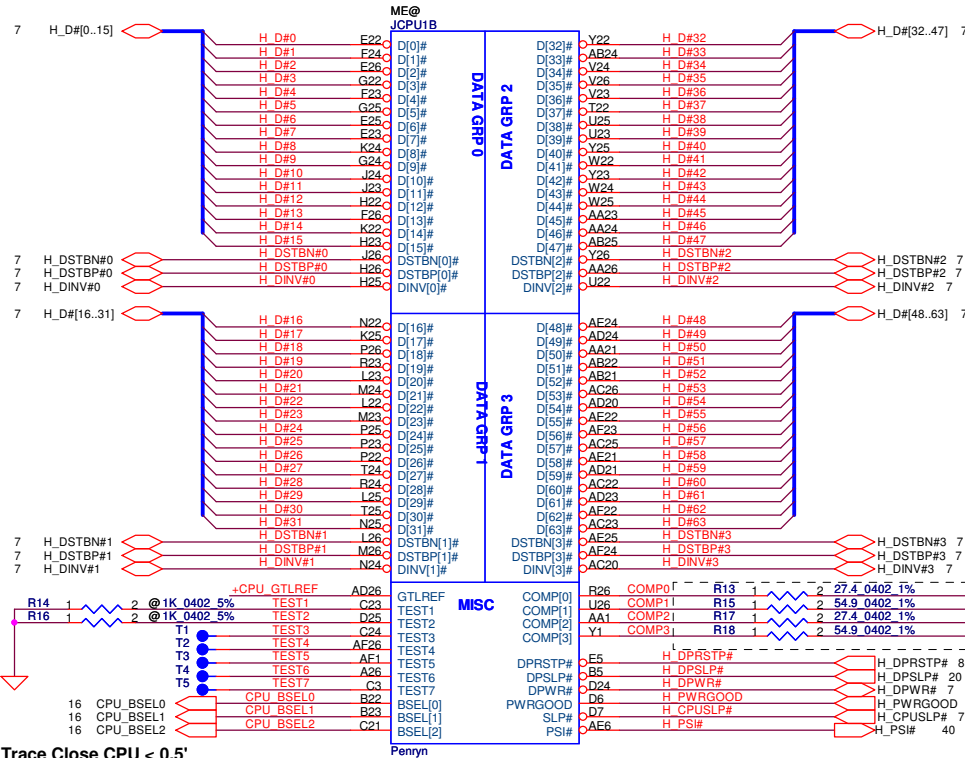


XDP Reserve for debug , Please close to CPU side



H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

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Trace Close CPU < 0.5'

Width=4 mil,
Spacing: 15mil
(55Ohm)

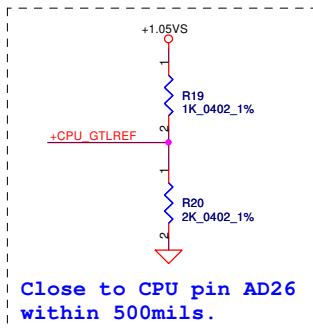
TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)

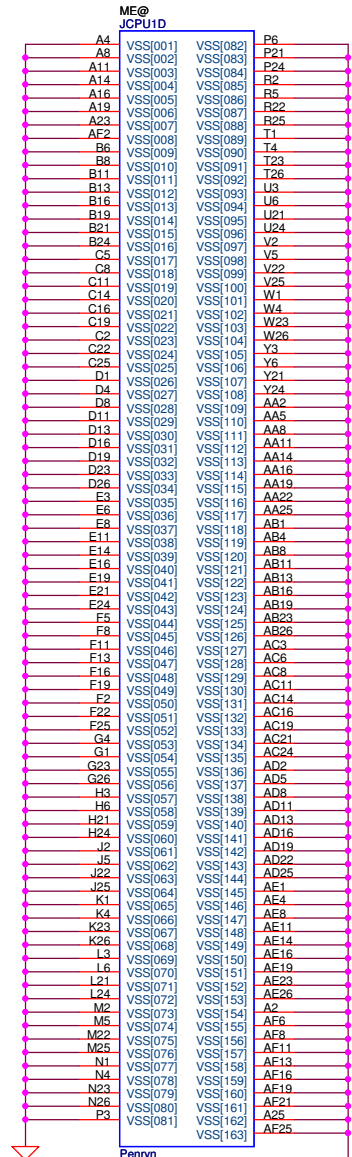
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

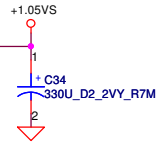
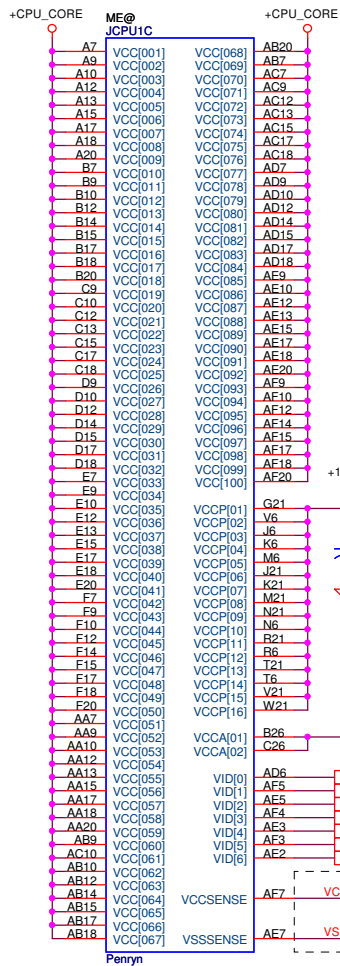
Layout note: Z0=55 ohm
0.5" max for GTLREF.



Close to CPU pin AD26
within 500mils.

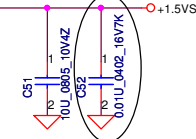


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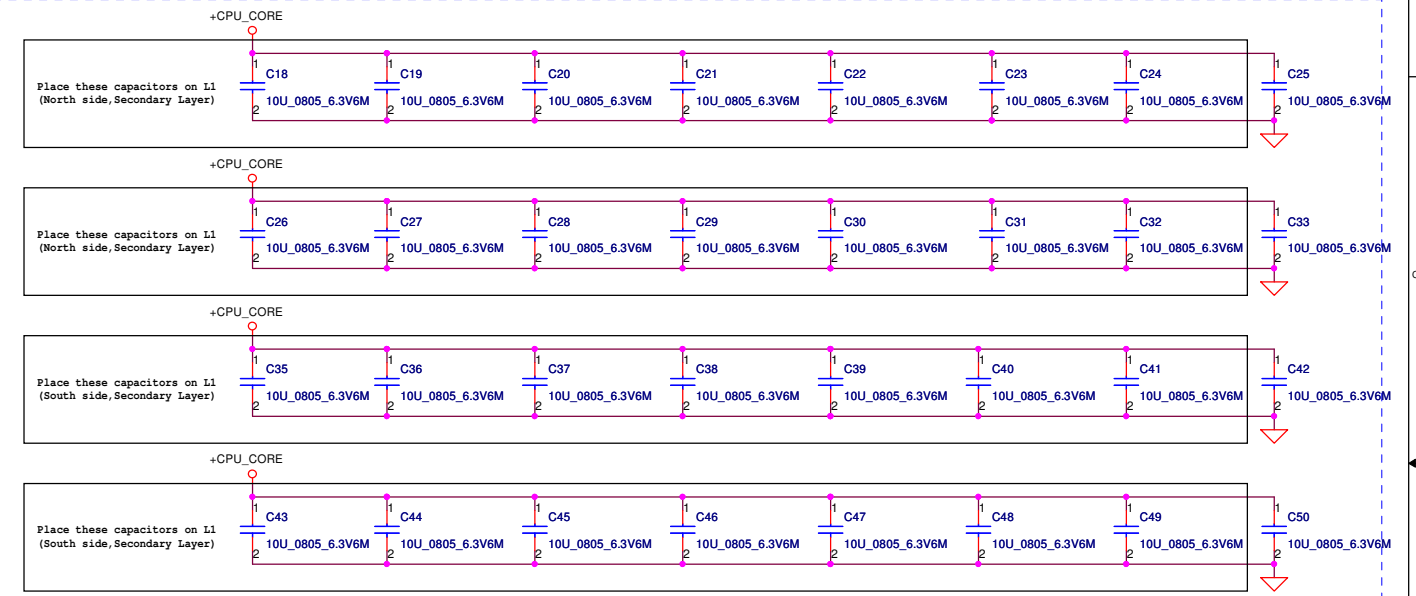
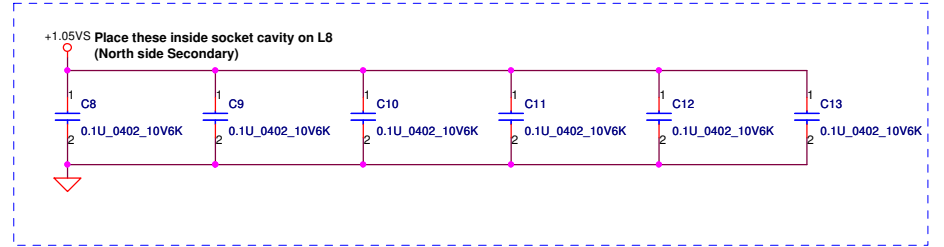
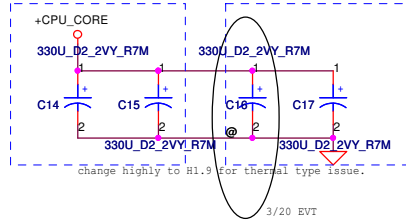
NEAR PIN B26

20mils

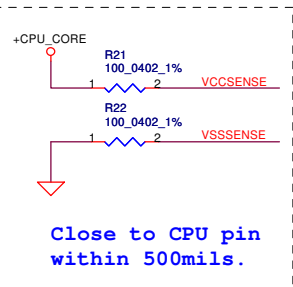


The trace width/space/other is 18/7/25.

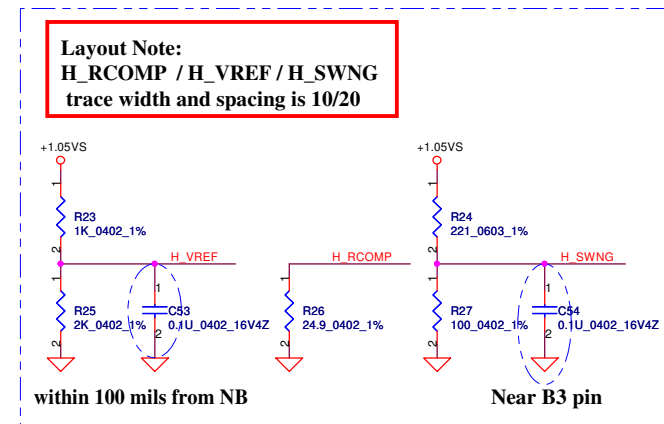
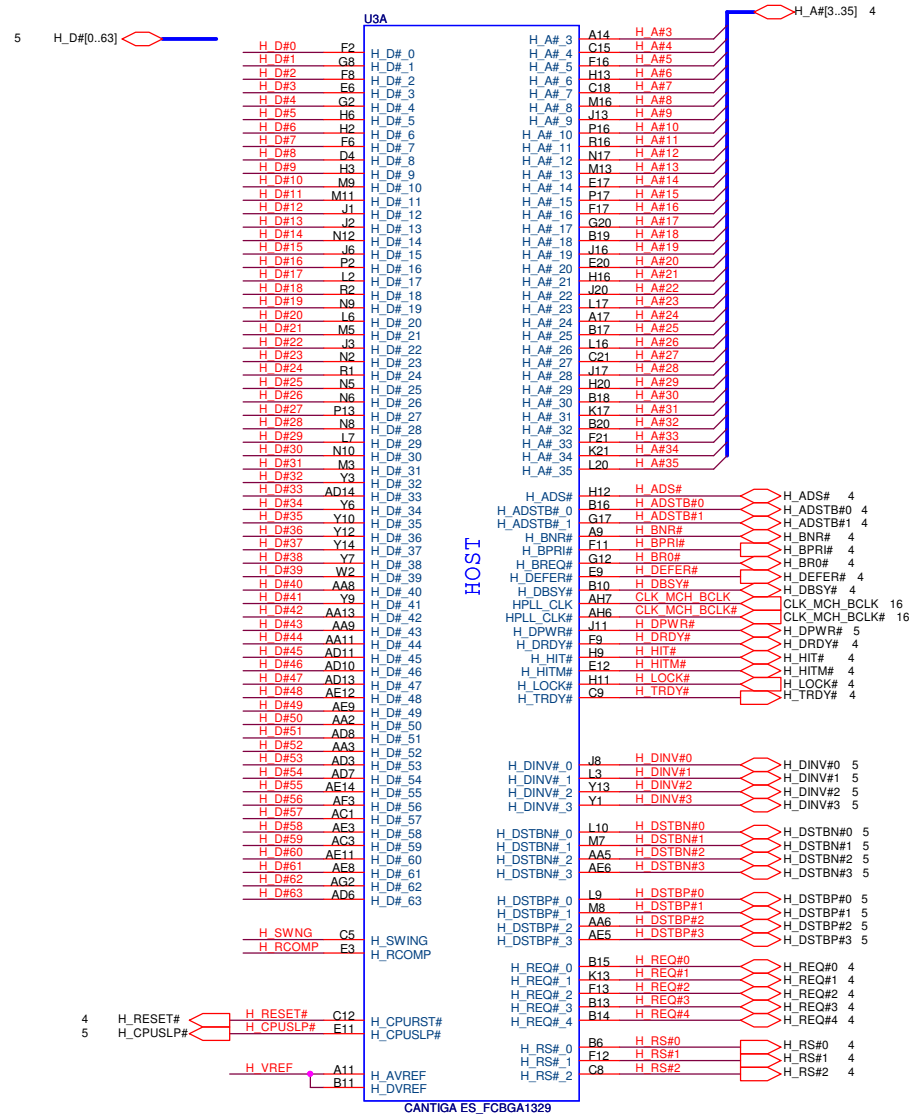
Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



Mid Frequency Decoupling

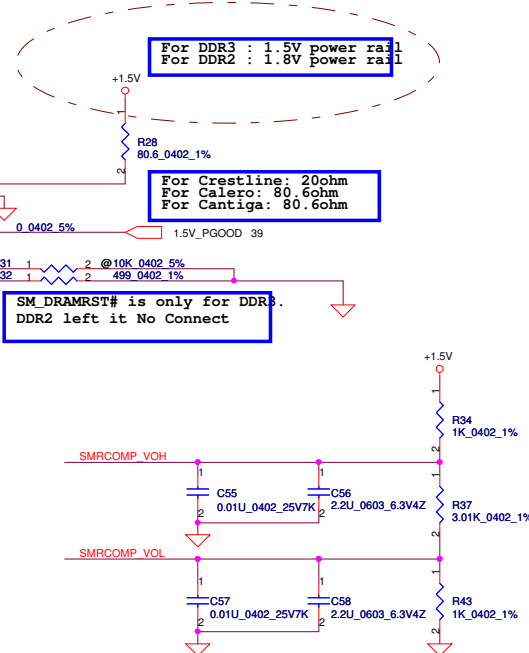
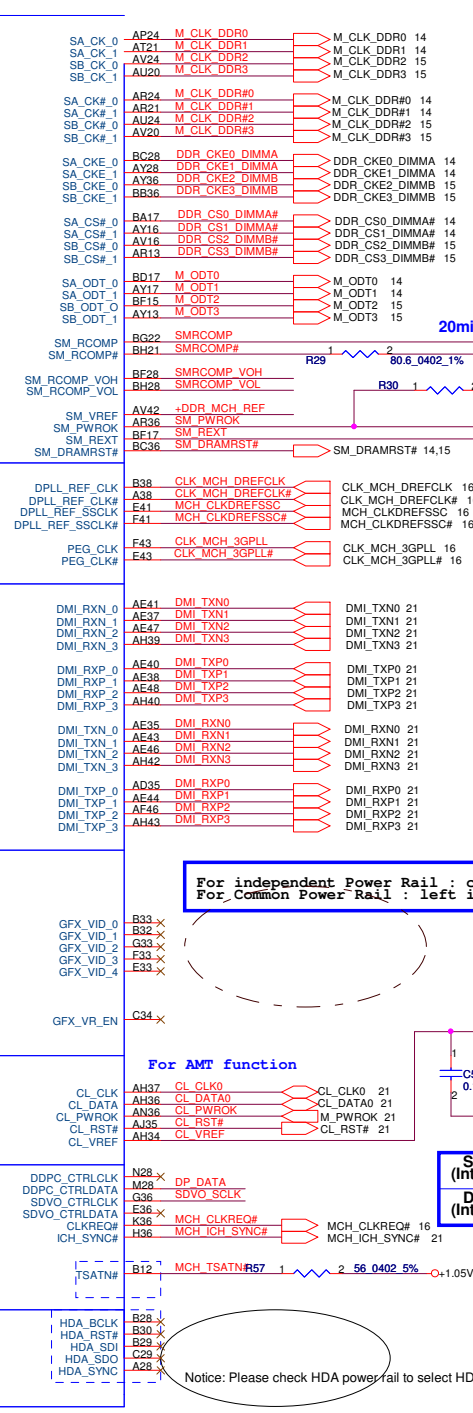
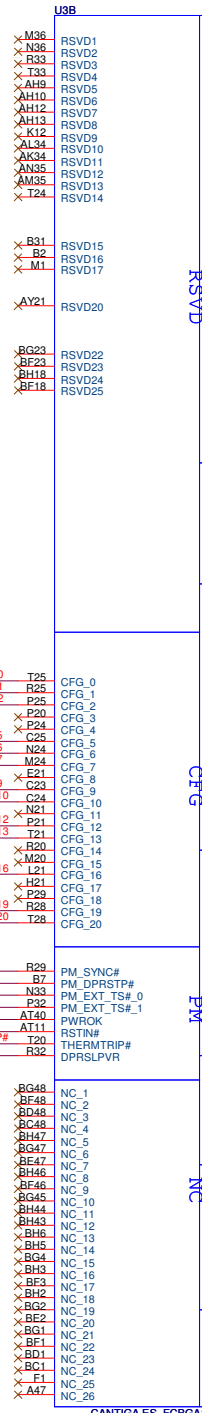
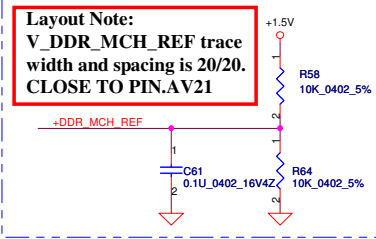
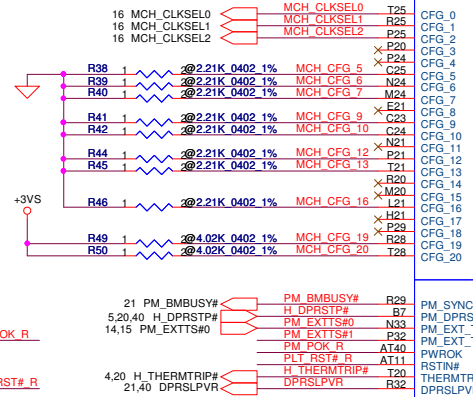
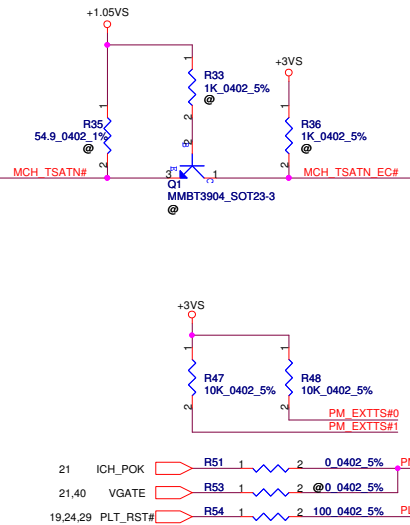


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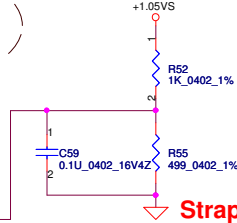


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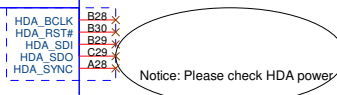
CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = ITPM Host Interface is enabled can support disble by SW. 1 = ITPM Host Interface is Disabled *(Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20	Internal pull-down (PCIE/SDVO select)	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.

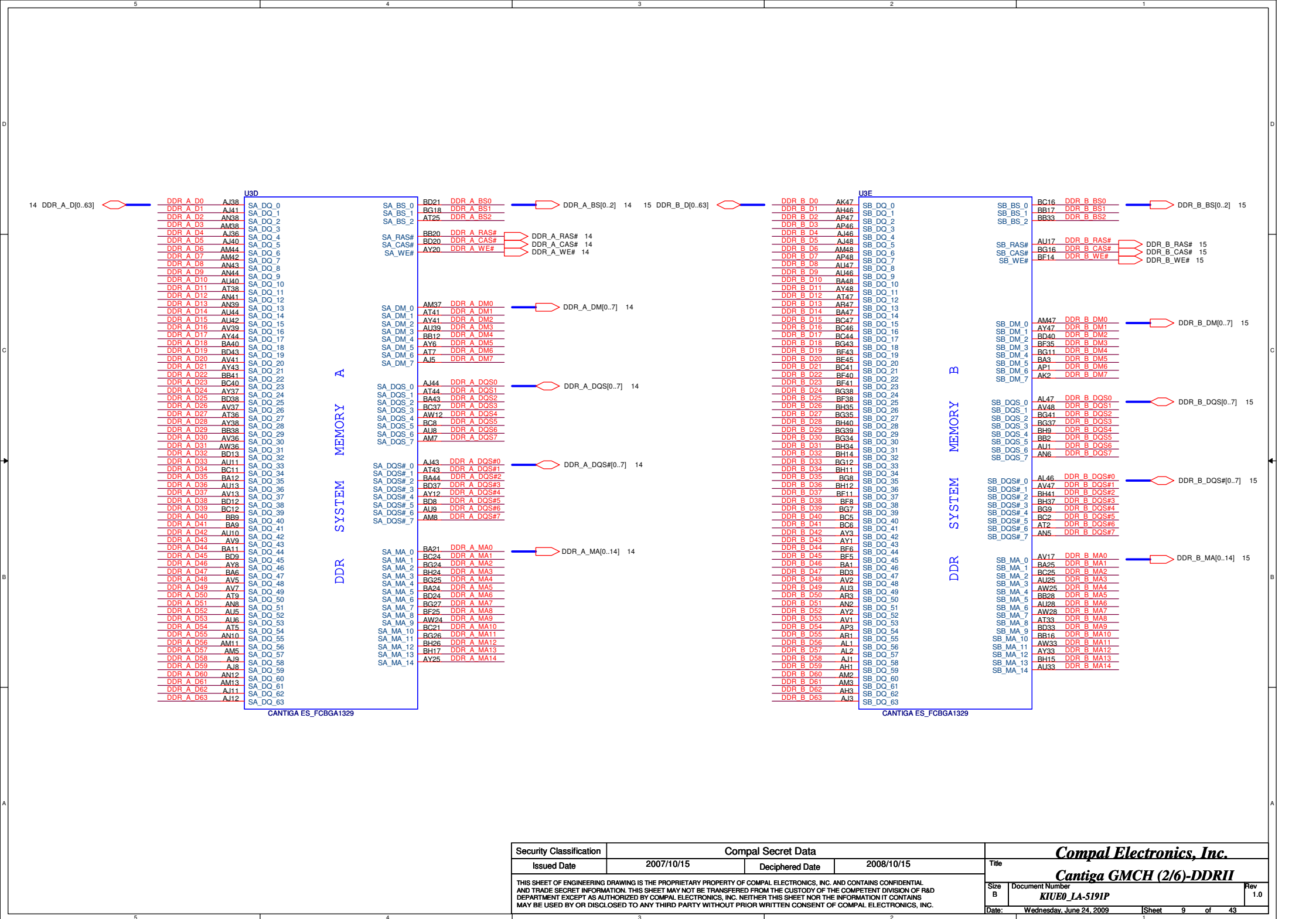


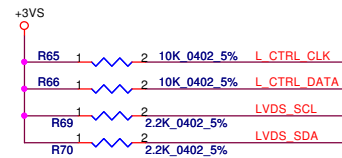
For independent Power Rail : connect to PWM CORE VDD
For Common Power Rail : left it No Connect



SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled * (Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled (Default) 1 = Digital display (iHDMI/DP) interface enabled



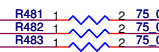
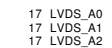
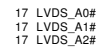
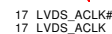
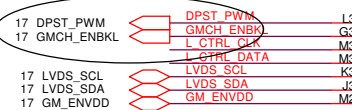




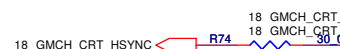
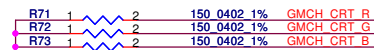
For Cantiga: 2.37kohm
For Crestline: 2.4kohm
For Calero: 1.5kohm

Note: All LVDS data signals/and it's compliments should be routed Differentially

EVT 0324 Reverse GMCH DPST



Layout Note: Place 150 Ω termination resistors close to GMCH



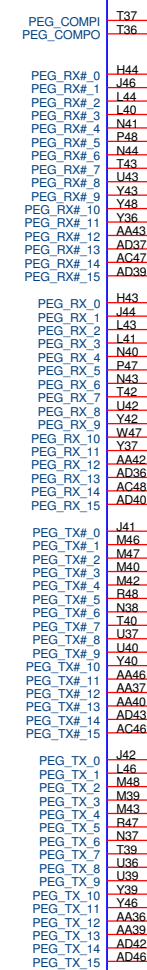
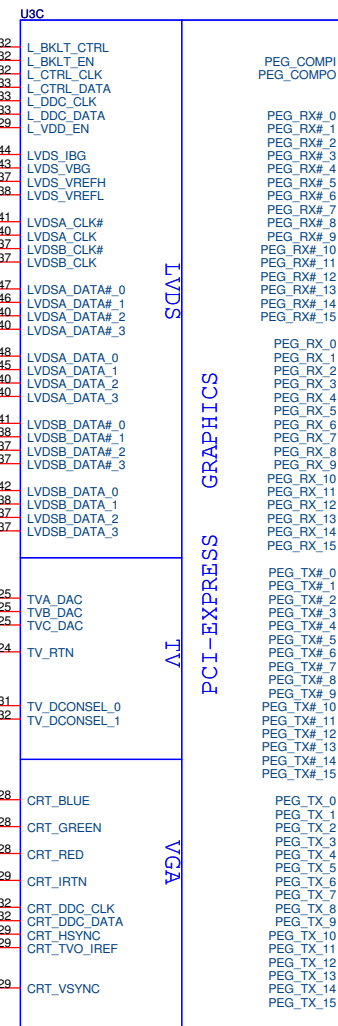
change R74,R75 from 33ohm to 30ohm
by checklist2.0 & CRB1.0 05/08/08

For Cantiga: 1.02kohm
For Crestline: 1.3kohm
For Calero: 255ohm

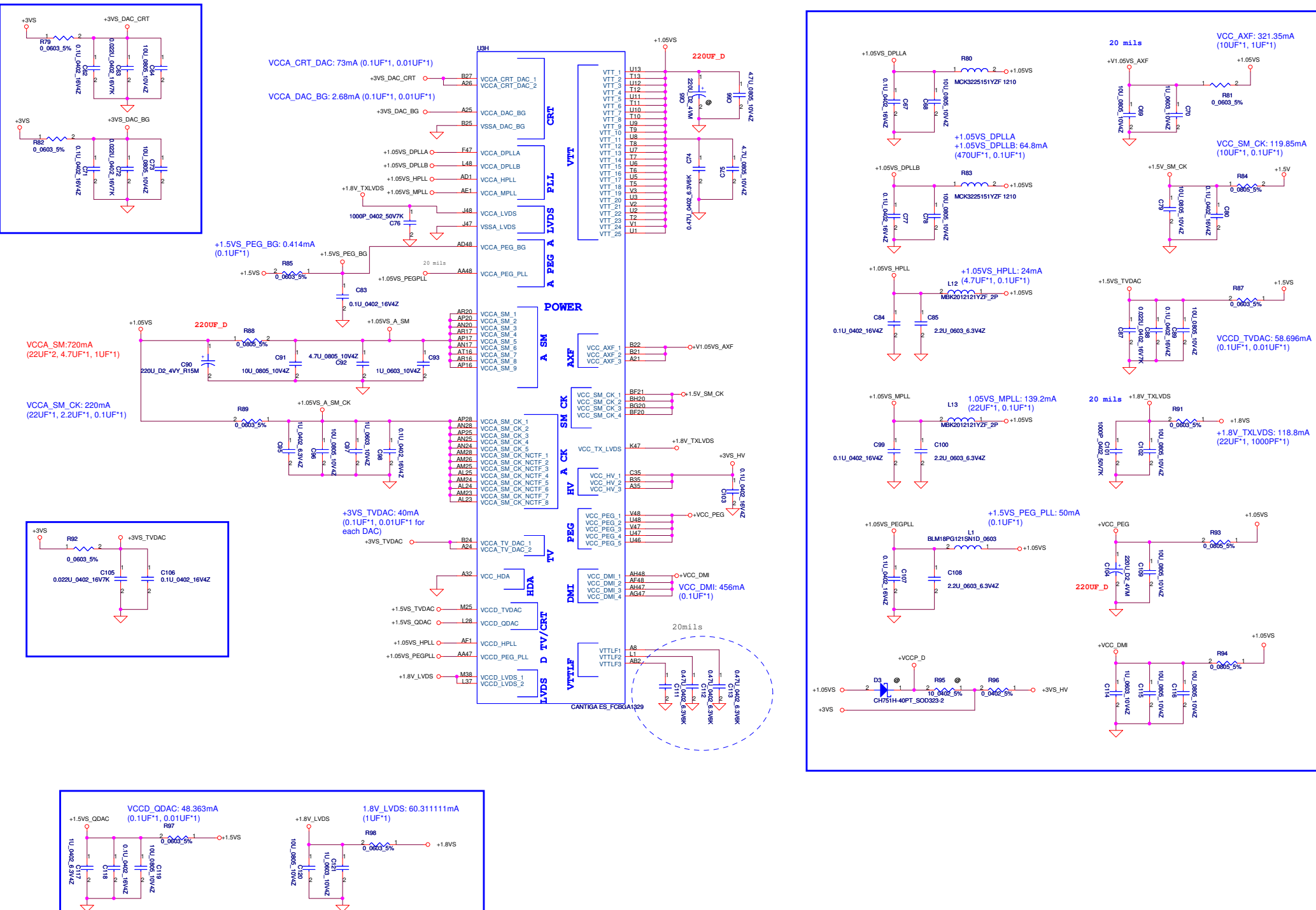
Place the resistor within 500mils
(1.27mm) of the (G)MCH
PEGCOMP trace width
and spacing is 20/25 mils.

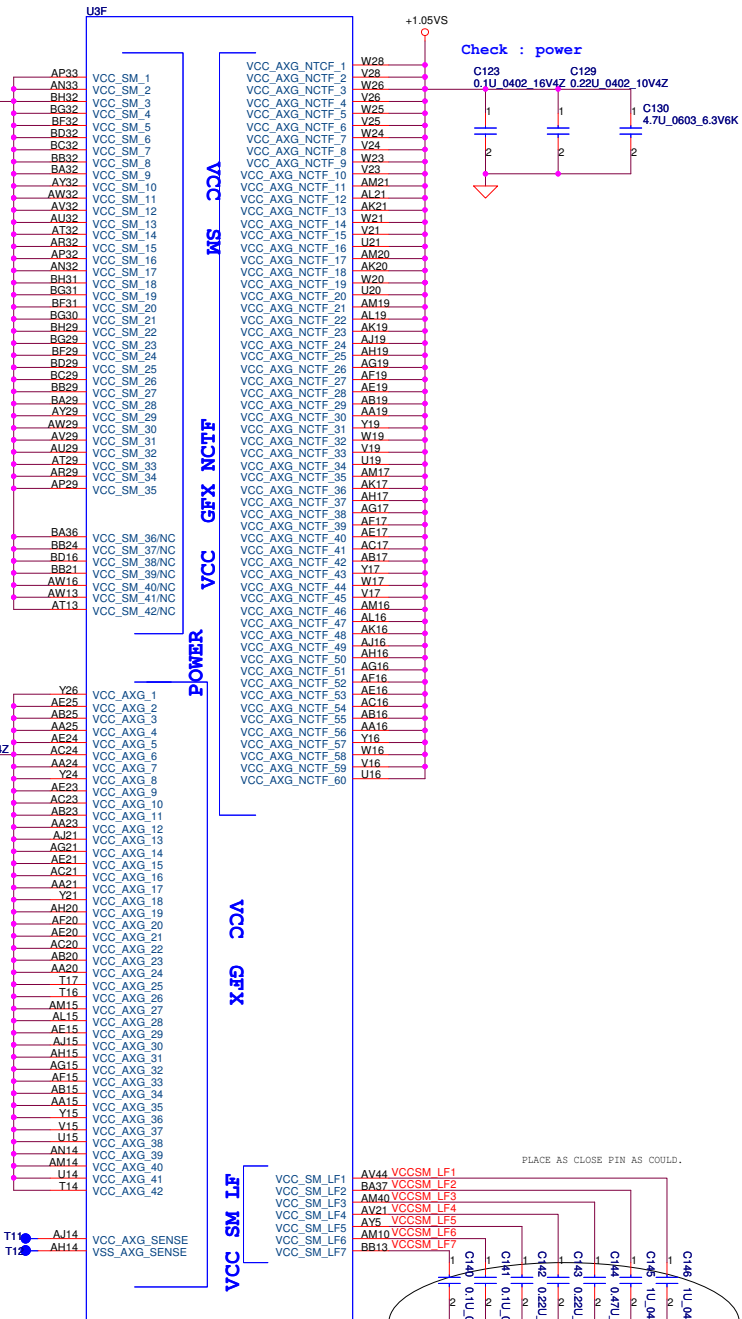
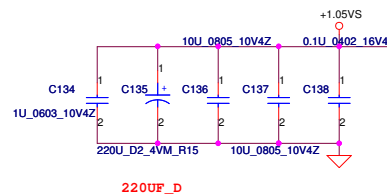
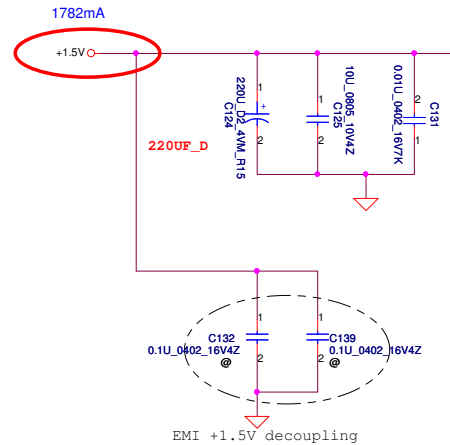
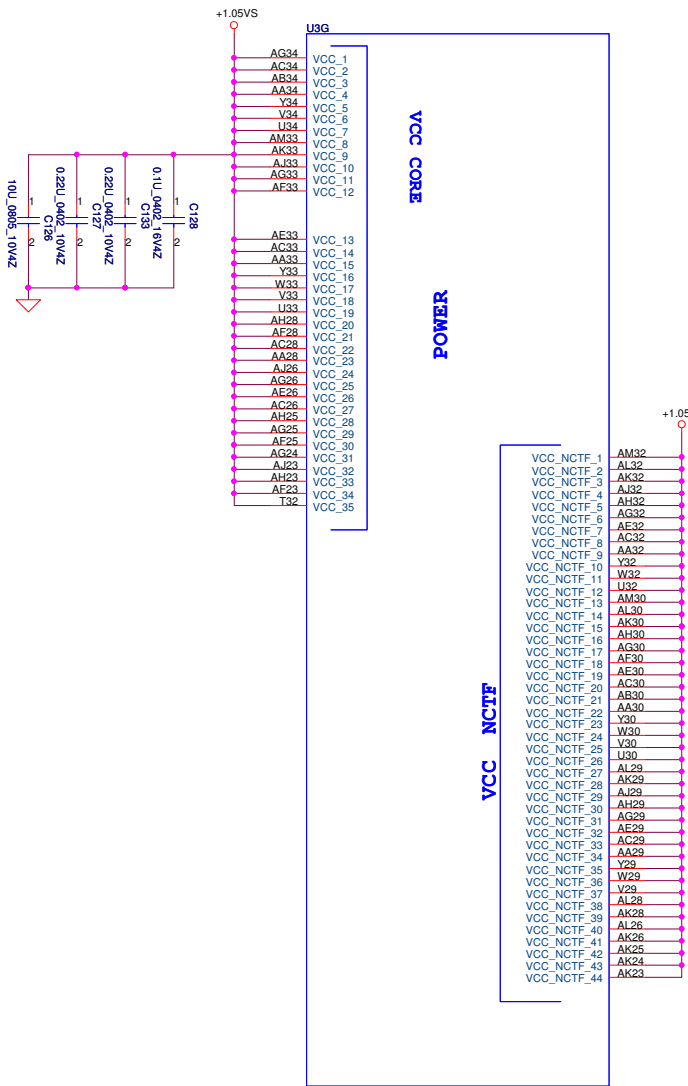


Please check Power source if want support IAMT



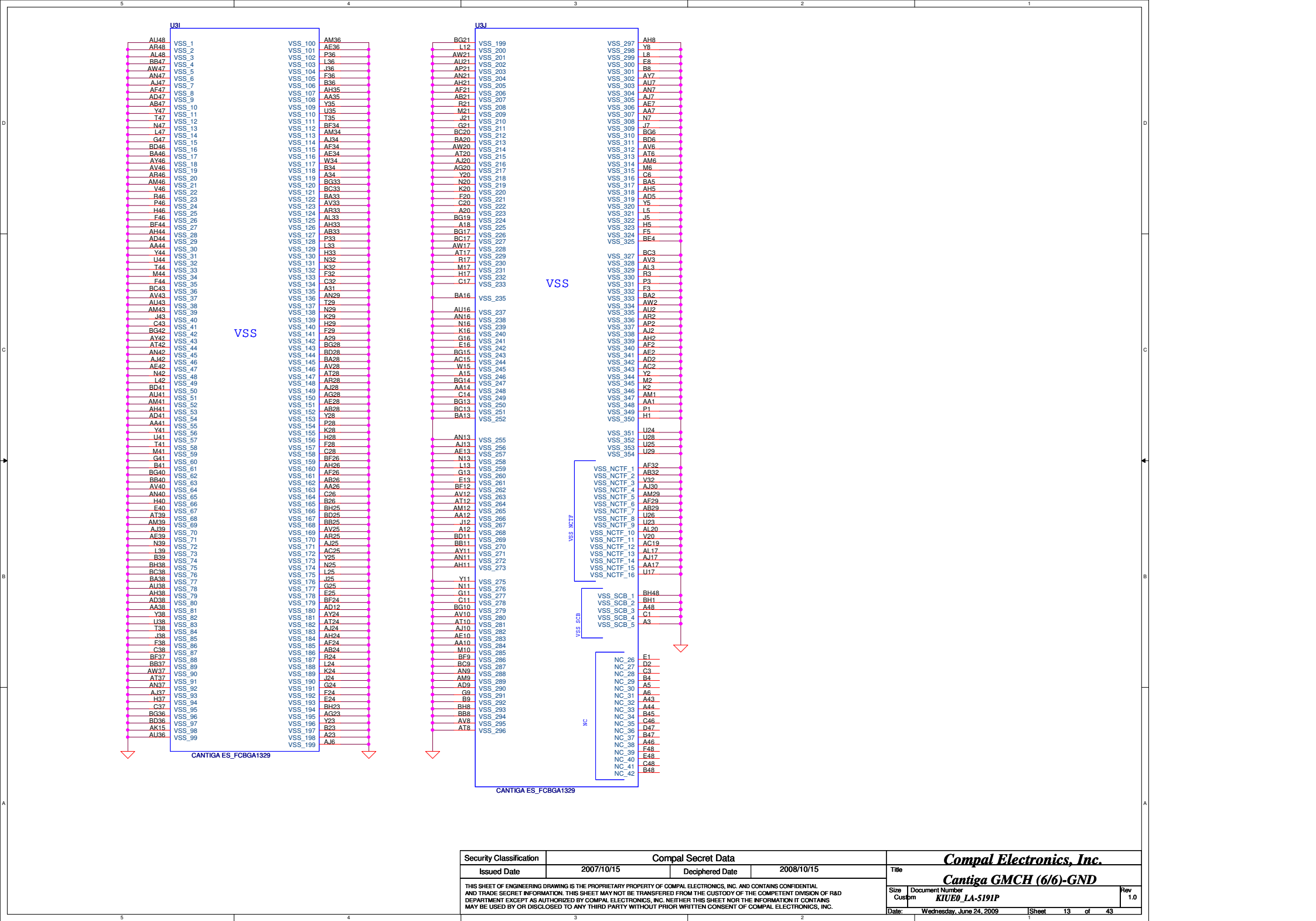
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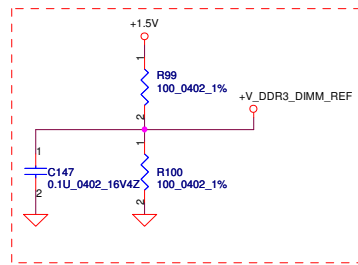
PLACE AS CLOSE PIN AS COULD.

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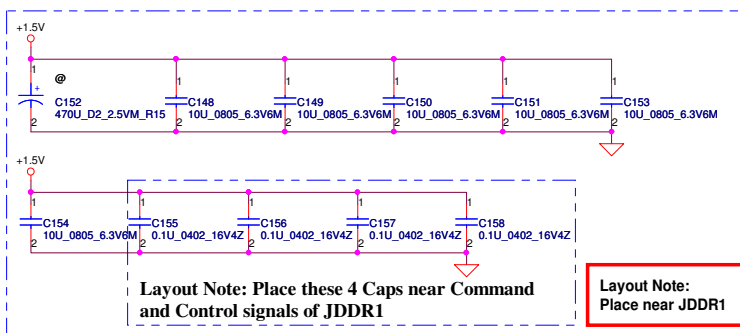
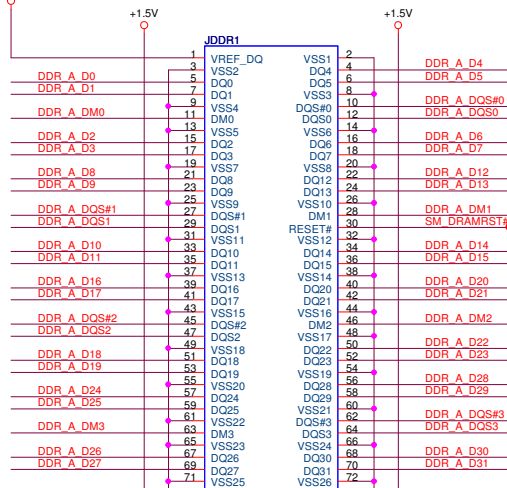


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Size	Document Number	Revision		1.0	
Custom	KIUE0 LA-5191P	Date		Wednesday, June 24, 2009	
Date		Sheet		13 of 43	

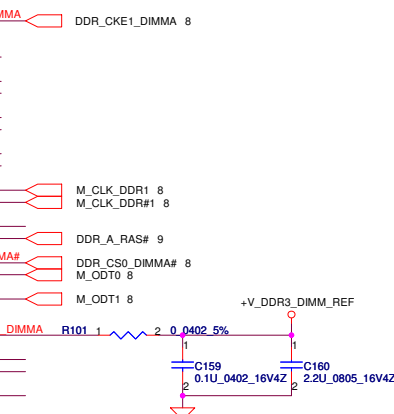
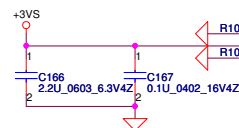
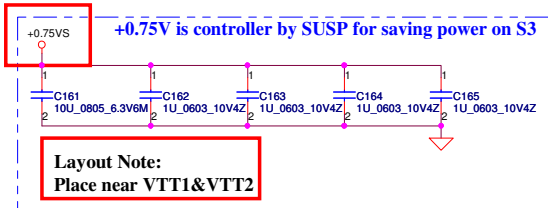
9 DDR_A_DQS#[0..7] 
 9 DDR_A_D#[0..63] 
 9 DDR_A_DM[0..7] 
 9 DDR_A_DQS#[0..7] 
 9 DDR_A_MA#[0..14] 
 9 DDR_A_BS[0..2] 



+V_DDR3_DIMM_REF

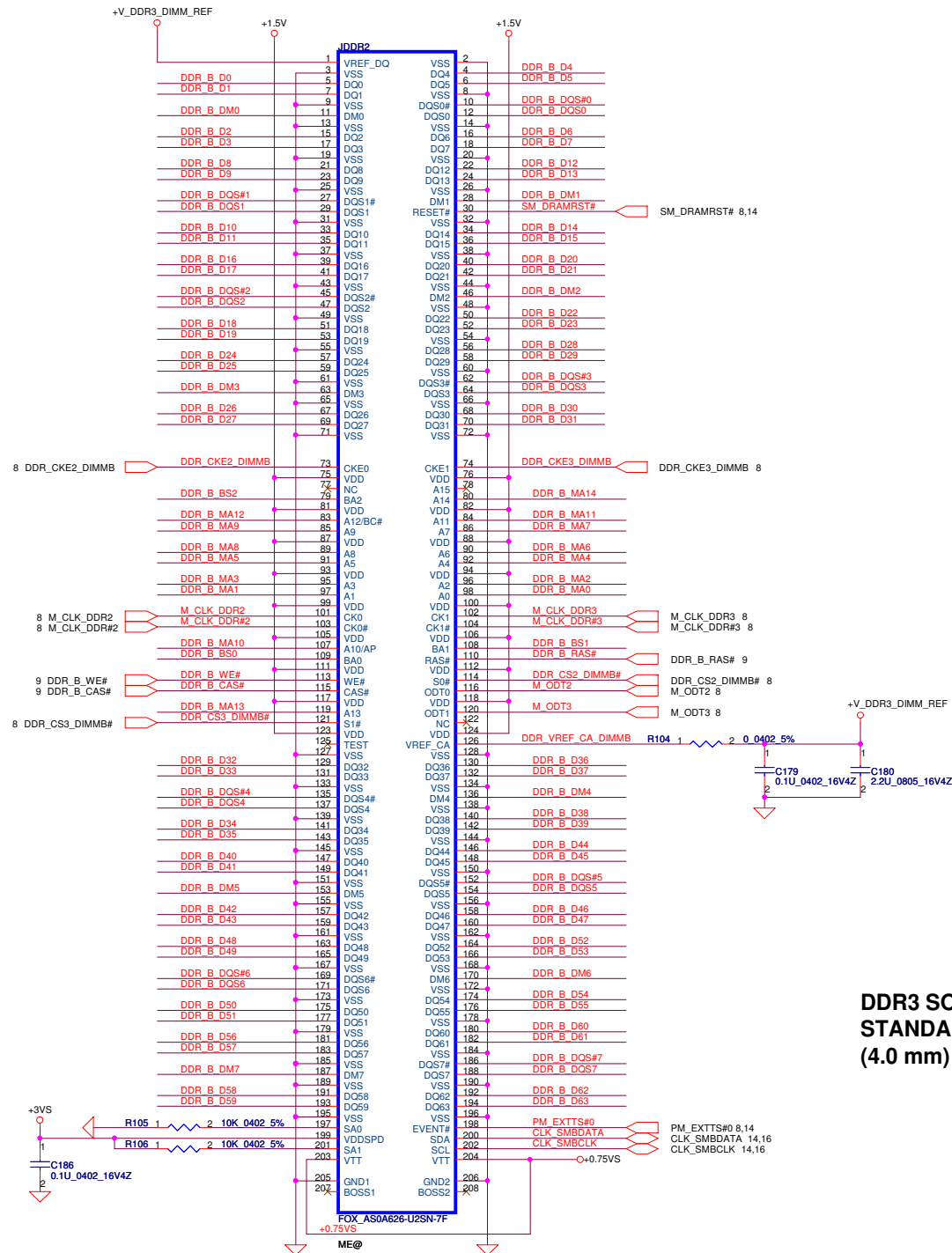
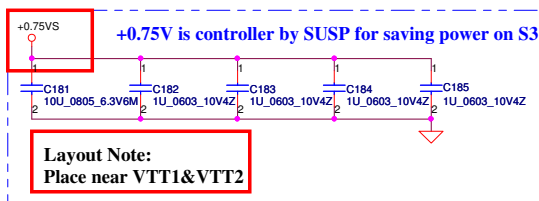
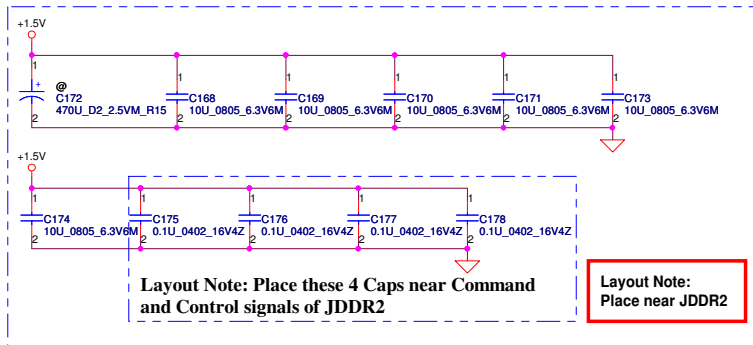
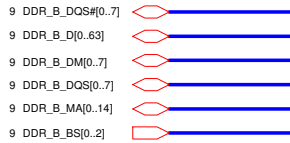


Layout Note:
Place near JDDR1



**DDR3 SO-DIMM A
REVERSE TYPE
(5.2mm)**

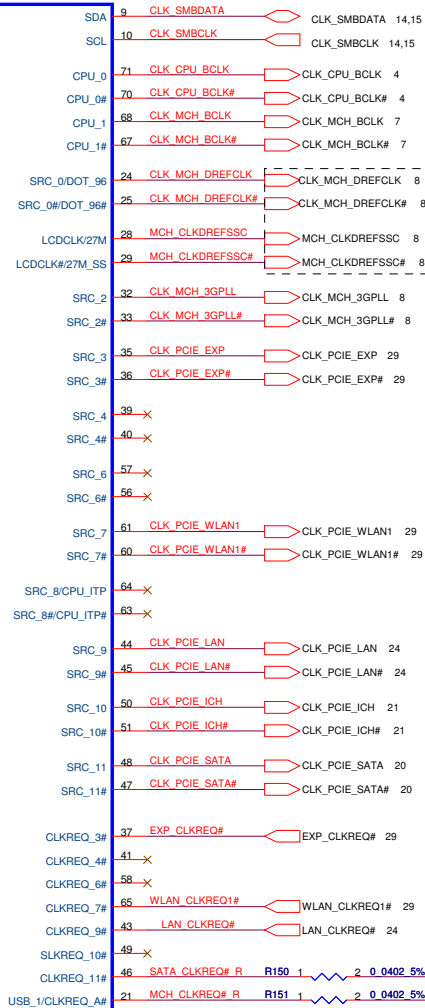
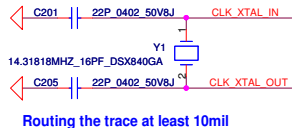
Security Classification				Compal Secret Data				Title			
Issued Date				2007/09/29				Deciphered Date			
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								DDR3-SODIMM SLOT1			
Size				Document Number				Rev			
Custor				KIUE0_LA-5191P				1.0			
Date				Wednesday, June 24, 2009				Sheet 14 of 43			



**DDR3 SO-DIMM B
STANDARD TYPE
(4.0 mm)**

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Issued Date				2007/09/29				Title			
				Deciphered Date				2007/09/29			
								Size			
								Document Number			
								KIUE0_LA-5191P			
								Rev			
								1.0			
								Date: Wednesday, June 24, 2009			
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ICH-SATA

Security Classification	Compal Secret Data			<i>Compal Electronics, Ltd.</i> Clock Generator CK505		
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title		
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				Custom	KIUE0_LA-5191P	1.0
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LCD POWER CIRCUIT

CMOS Camera POWER CIRCUIT

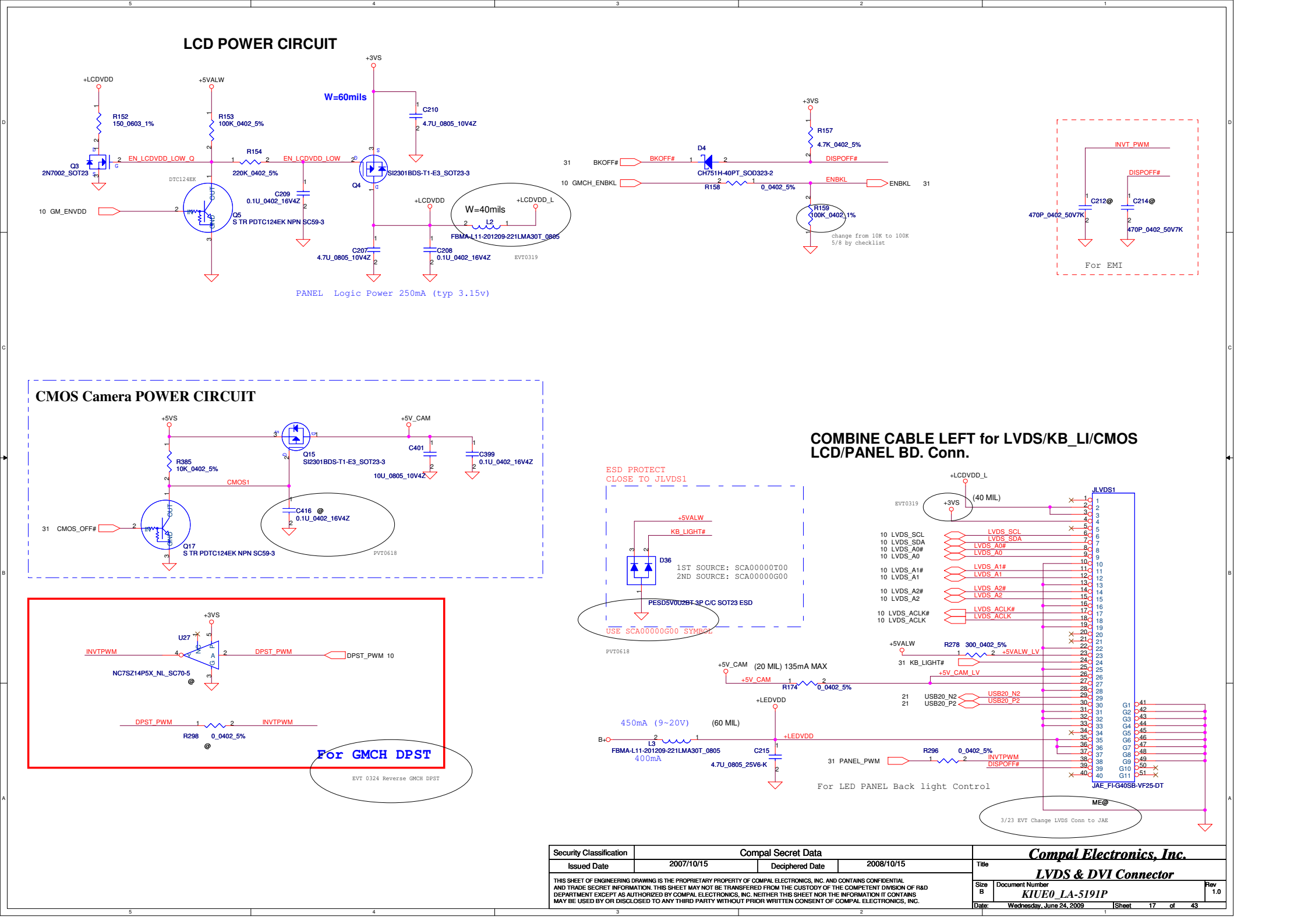
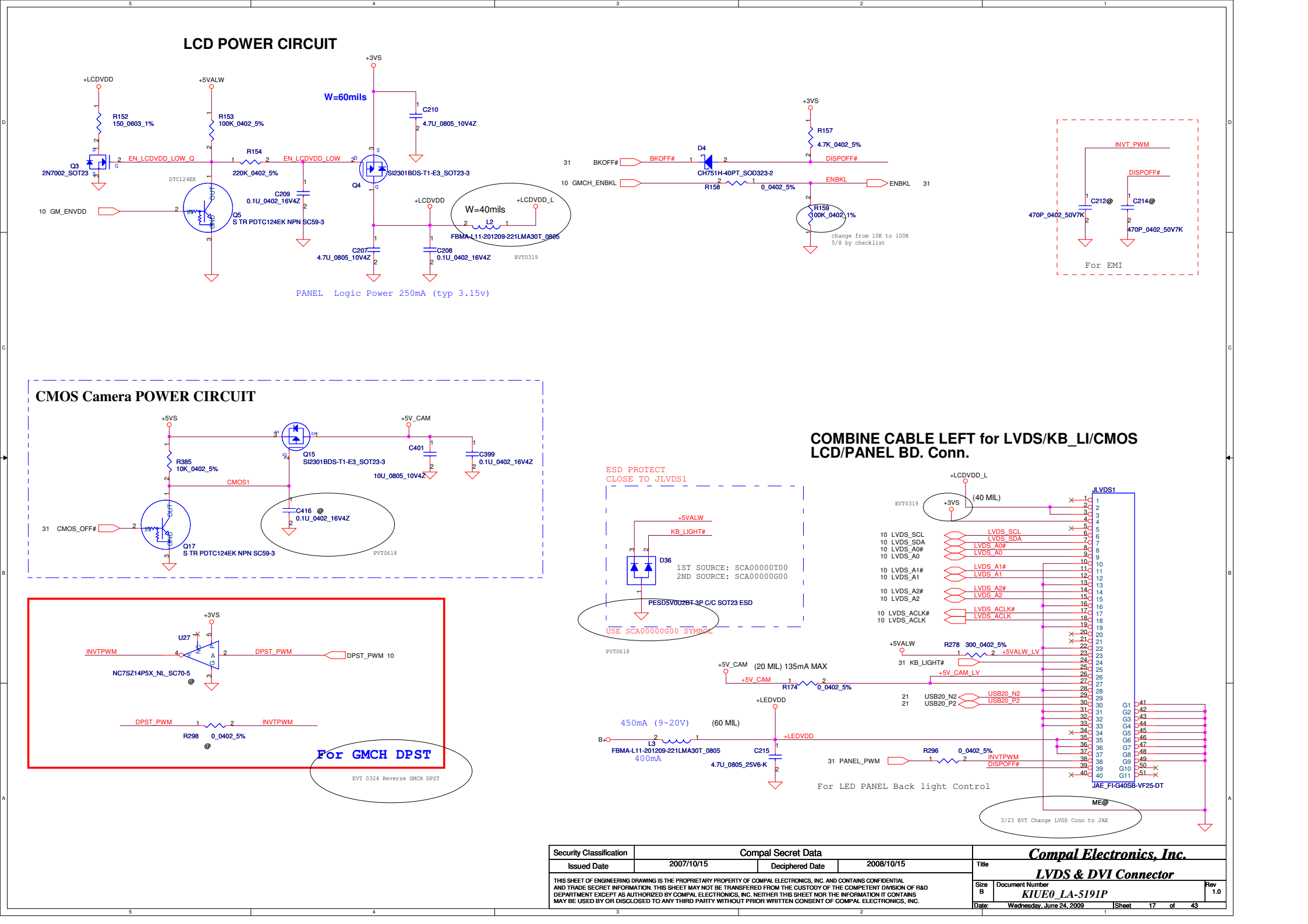
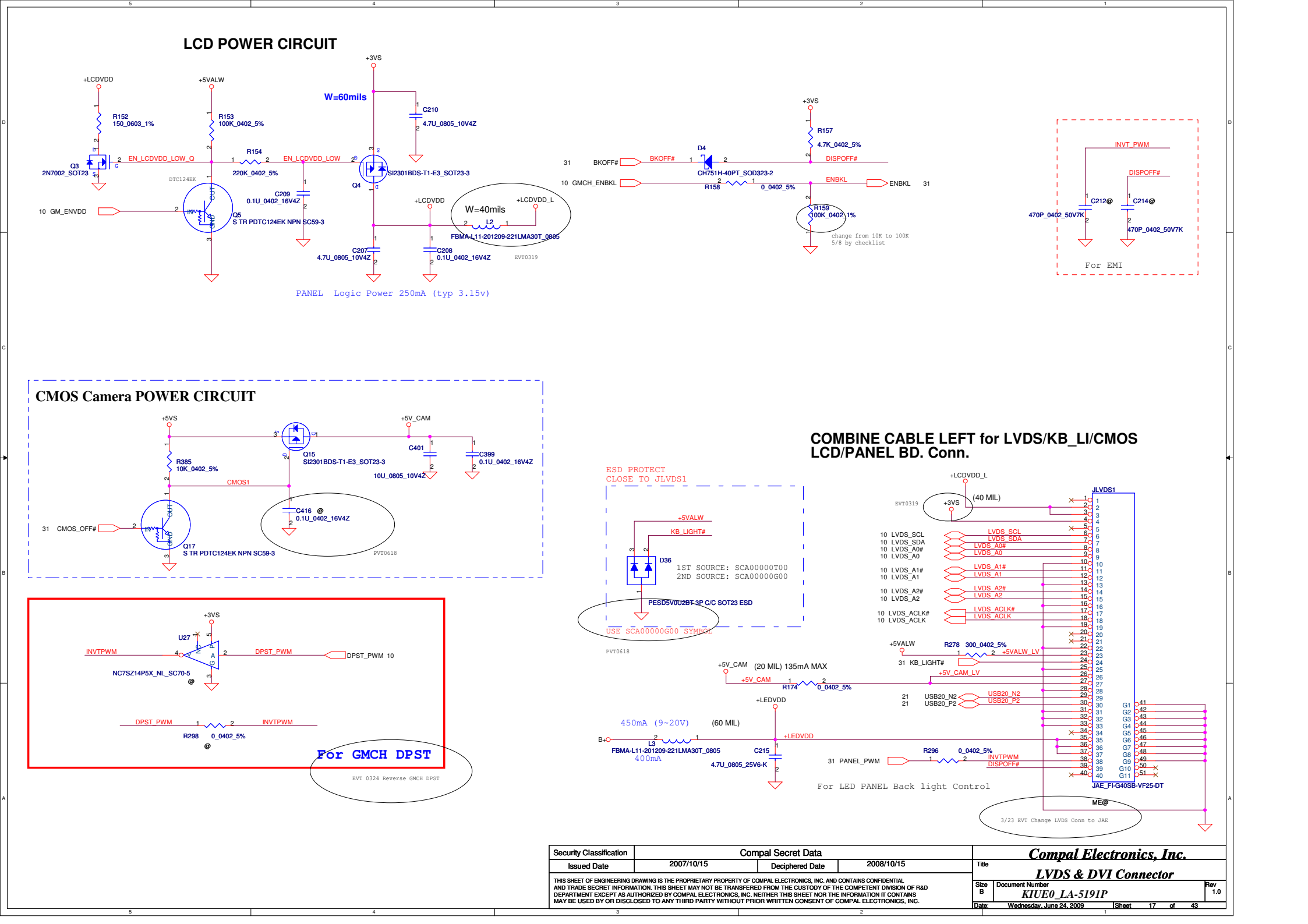
COMBINE CABLE LEFT for LVDS/KB_LI/CMOS LCD/PANEL BD. Conn.

Security Classification

Security Classification	Compal Secret Data
Issued Date	2007/10/15
Deciphered Date	2008/10/15

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Compal Electronics, Inc.
LVDS & DVI Connector
 Title: **KIUE0_LA-5191P**
 Date: Wednesday, June 24, 2009
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LCD POWER CIRCUIT

CMOS Camera POWER CIRCUIT

COMBINE CABLE LEFT for LVDS/KB_LI/CMOS LCD/PANEL BD. Conn.

Security Classification

Security Classification	Compal Secret Data
Issued Date	2007/10/15
Deciphered Date	2008/10/15

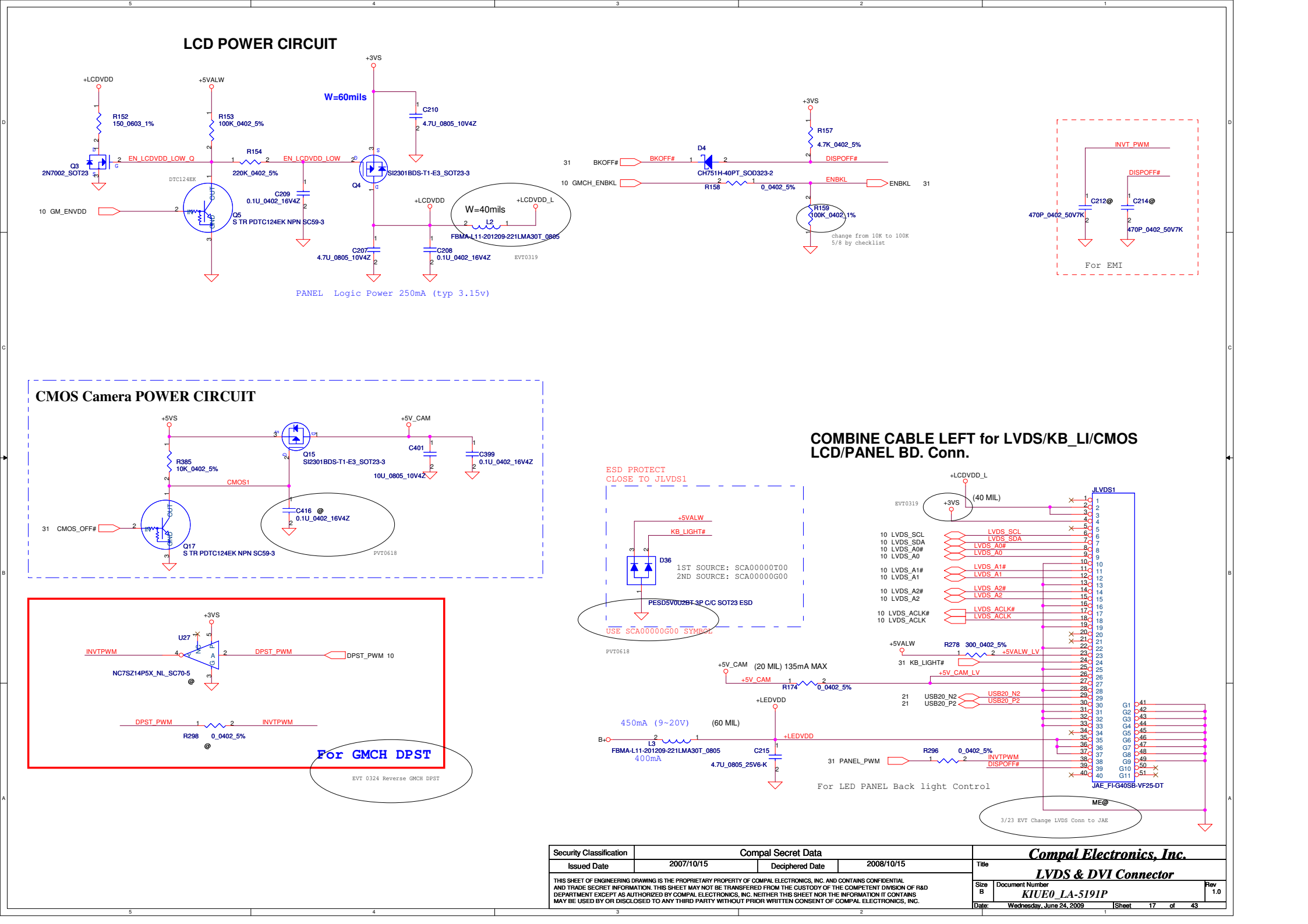
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Compal Electronics, Inc.

LVDS & DVI Connector

Document Number
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LCD POWER CIRCUIT

W=60mils

W=40mils

PANEL Logic Power 250mA (typ 3.15v)

change from 10K to 100K
5/8 by checklist

For EMI

CMOS Camera POWER CIRCUIT

PVT0618

COMBINE CABLE LEFT for LVDS/KB_LI/CMOS LCD/PANEL BD. Conn.

ESD PROTECT
CLOSE TO JLVDS1

1ST SOURCE: SCA00000T00
2ND SOURCE: SCA00000G00

USE SCA00000G00 SYMBOL

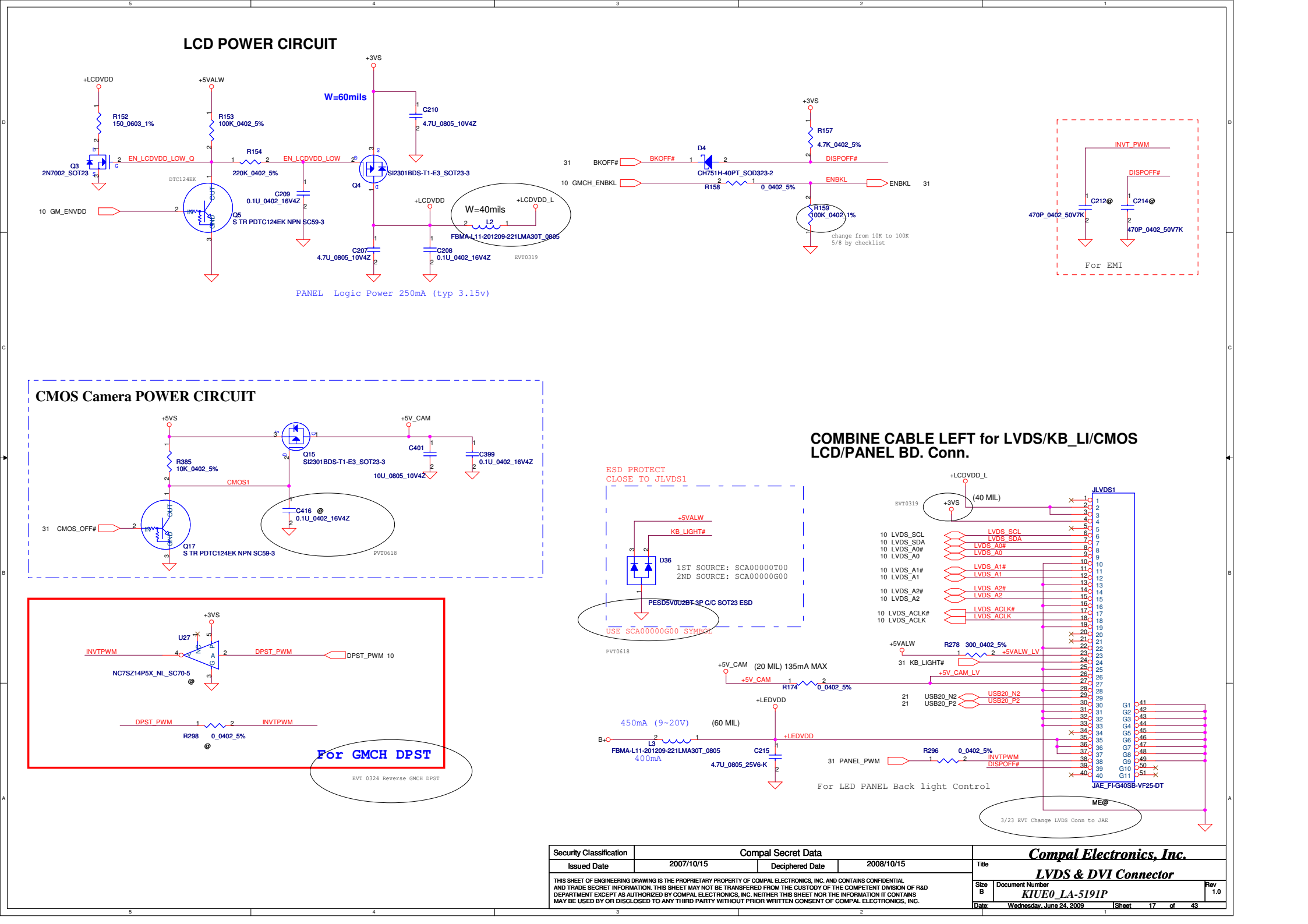
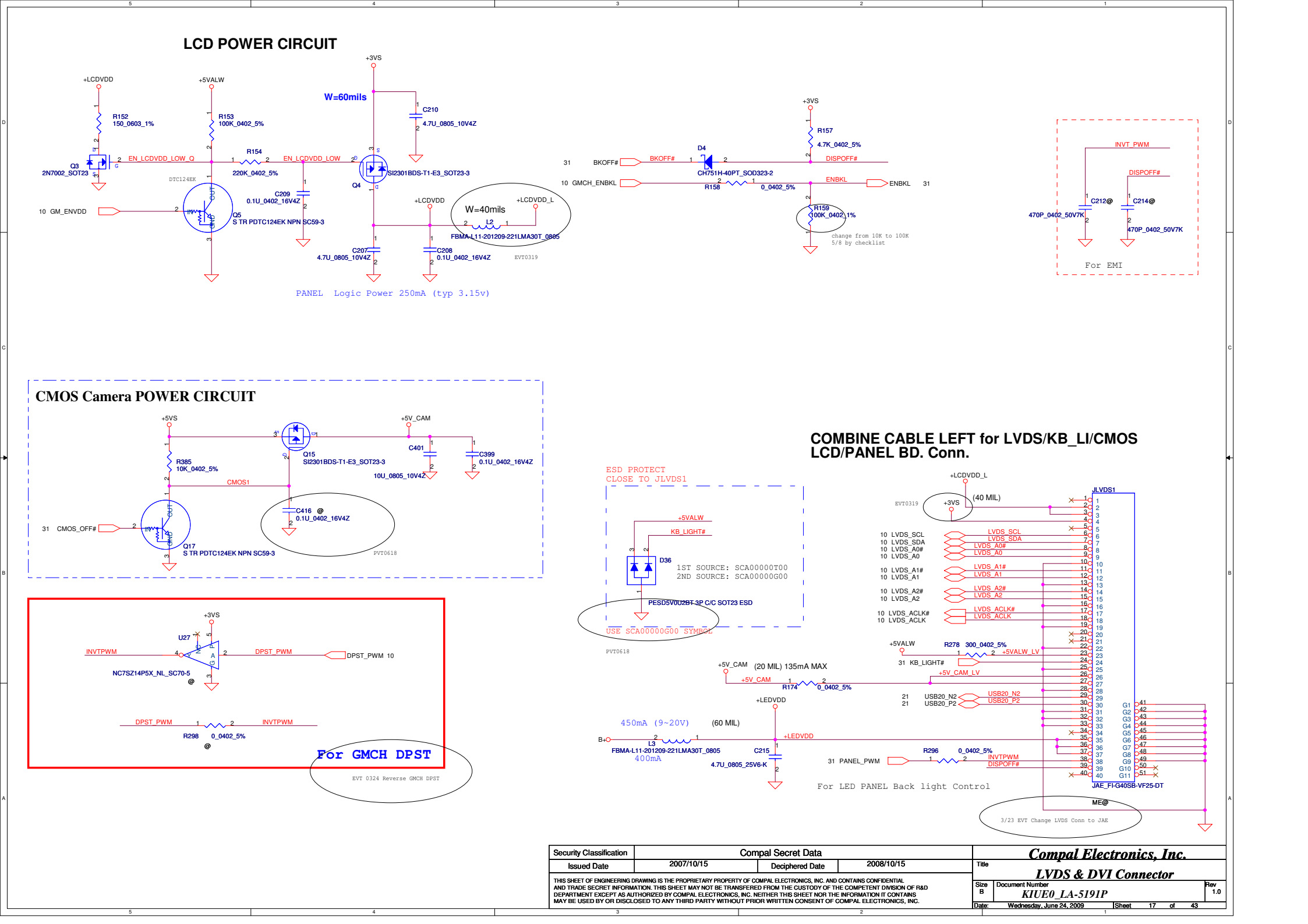
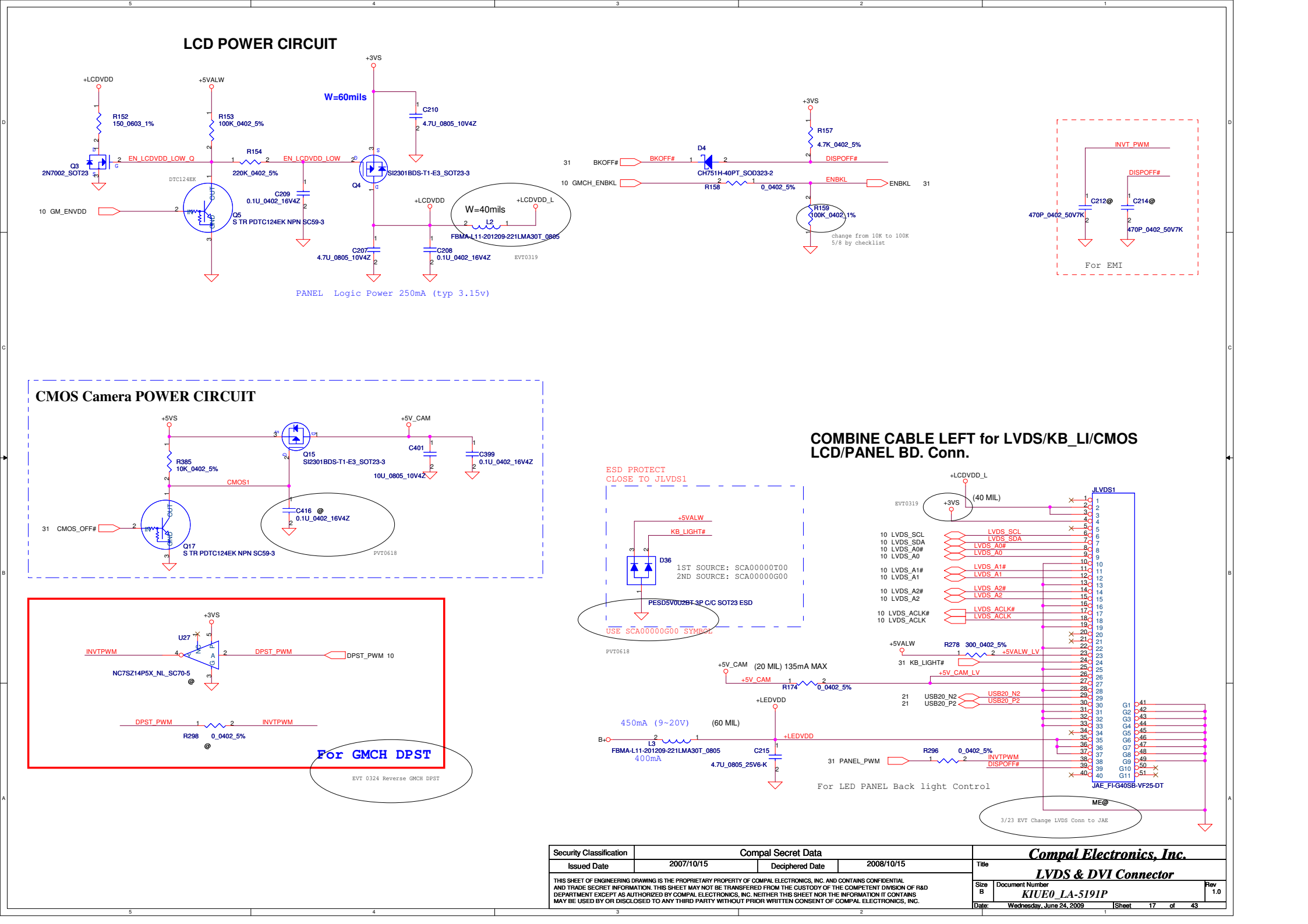
PVT0618

3/23 EVT Change LVDS Conn to JAE

For GMCH DPST

EVT 0324 Reverse GMCH DPST

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				Size B	Document Number
				KIUE0_LA-5191P	
Date: Wednesday, June 24, 2009				Sheet 17	of 43



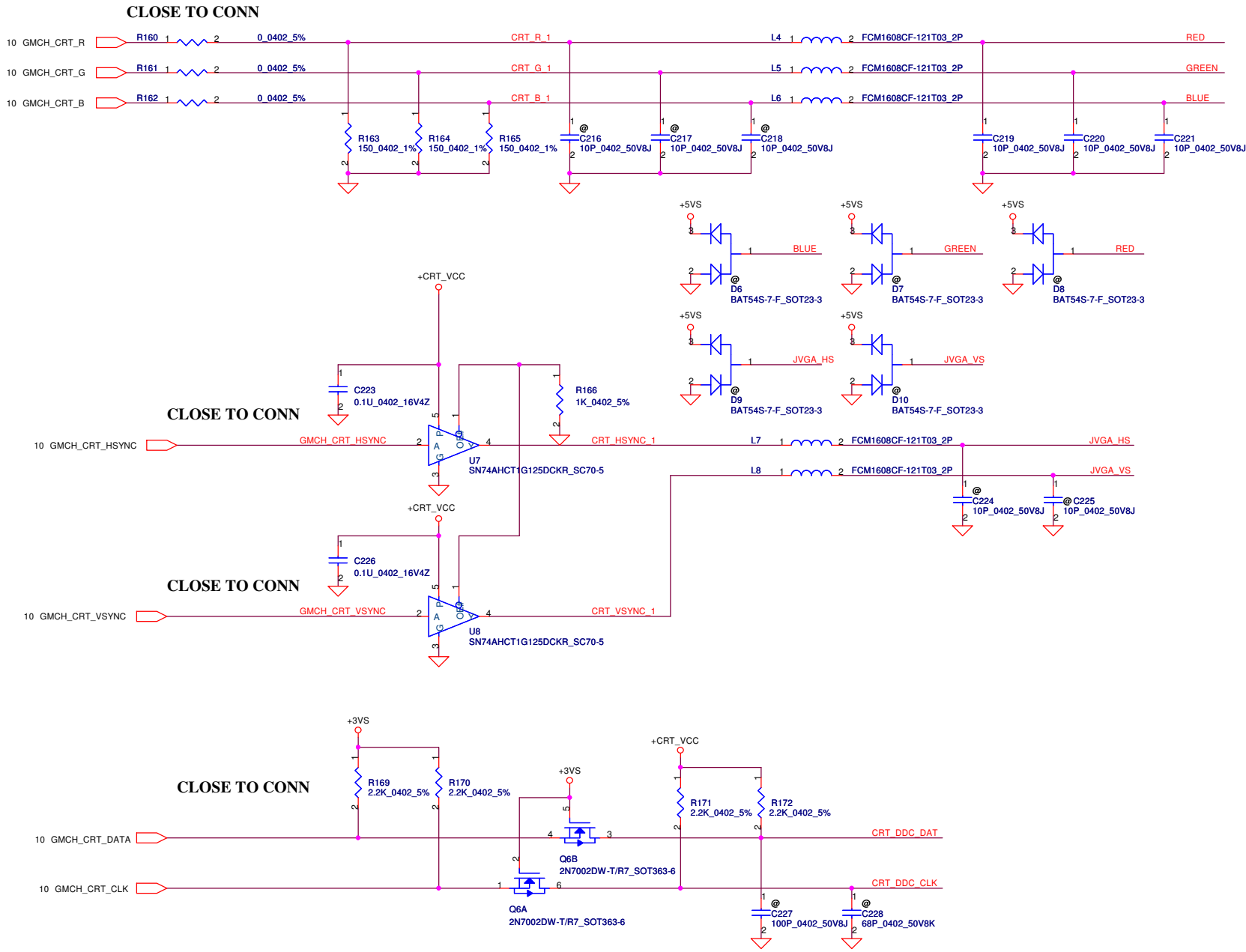
LCD POWER CIRCUIT

CMOS Camera POWER CIRCUIT

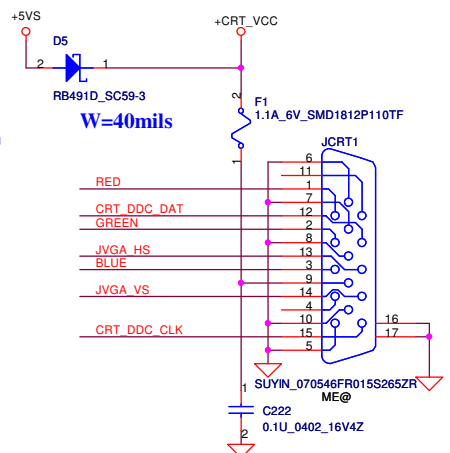
COMBINE CABLE LEFT for LVDS/KB_LI/CMOS LCD/PANEL BD. Conn.

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Size B	Rev 1.0	Sheet 17 of 43	

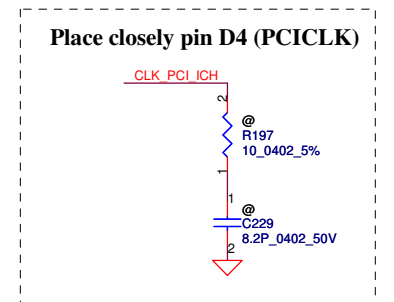
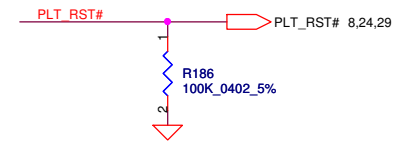
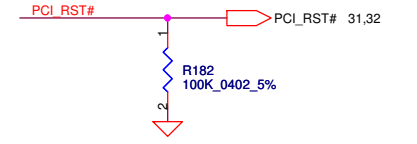
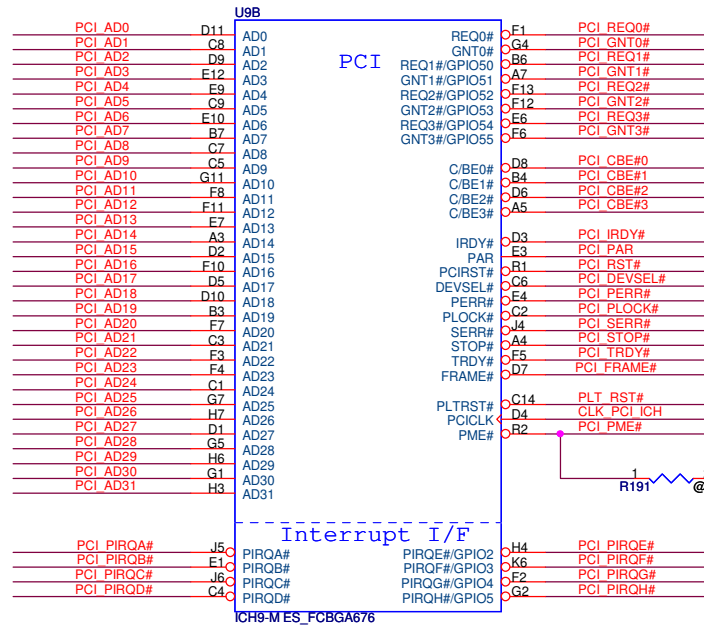
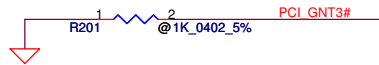
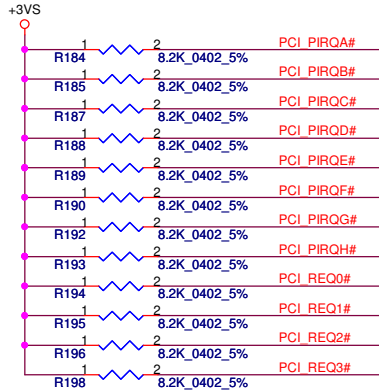
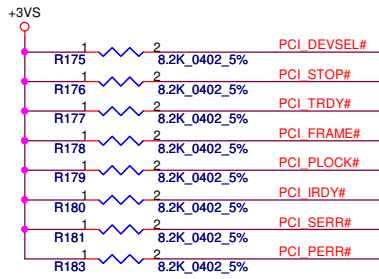


CRT Connector



PIN ASSIGMENT

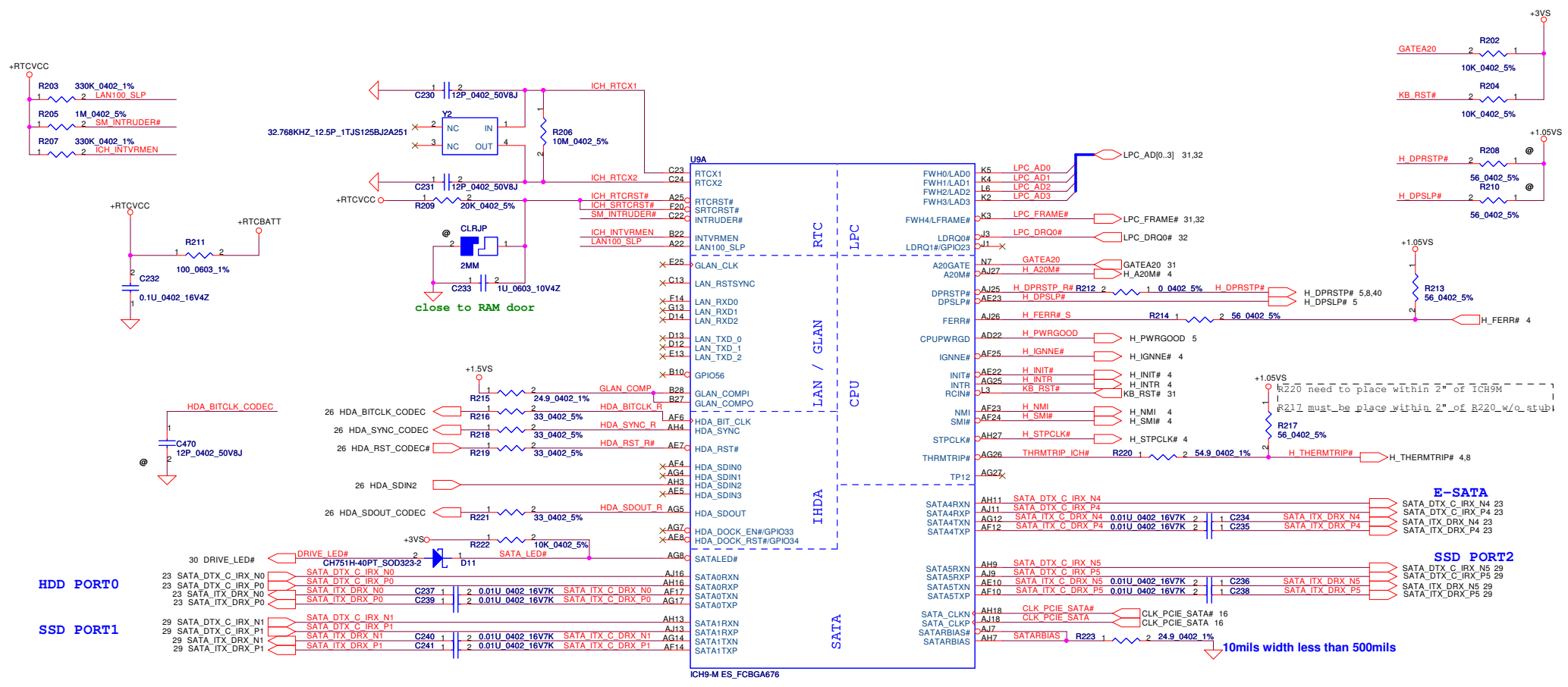
D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

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Size		Document Number		Rev	
		KIU00_LA-5191P		1.0	
Date:		Wednesday, June 24, 2009		Sheet 19 of 43	



HDD PORT0

SSD PORT1

E-SATA

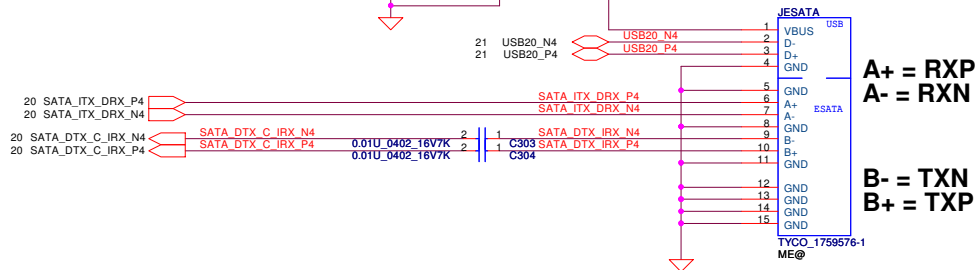
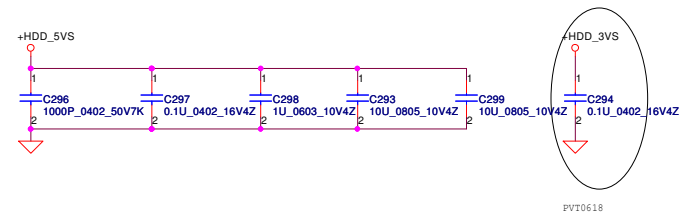
SSD PORT2

Need check

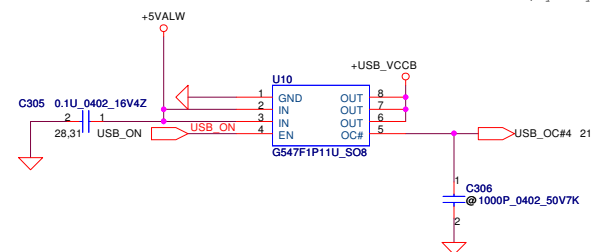
XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

SATA PORT LIST	
PORT	DEVICE
0	HDD
1	Mini-Card SSD PORT1
4	E-SATA
5	Mini-Card SSD PORT2

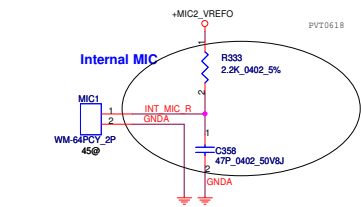
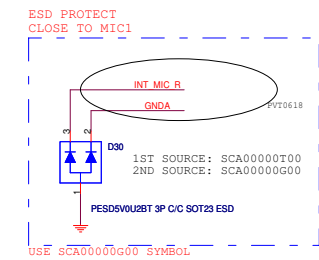
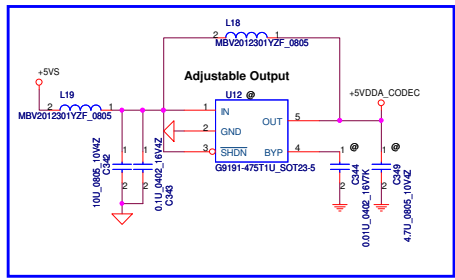


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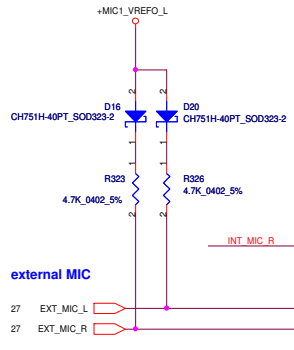
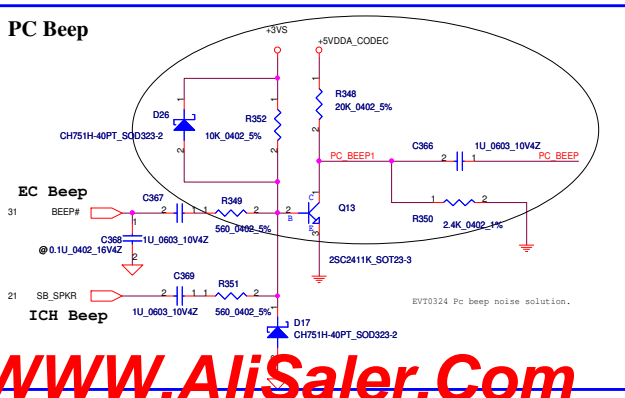
3/26 Remove ESD Diode ,by AndyYL



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						HDD & ODD Connector		
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						Date	Wednesday, June 24, 2009	



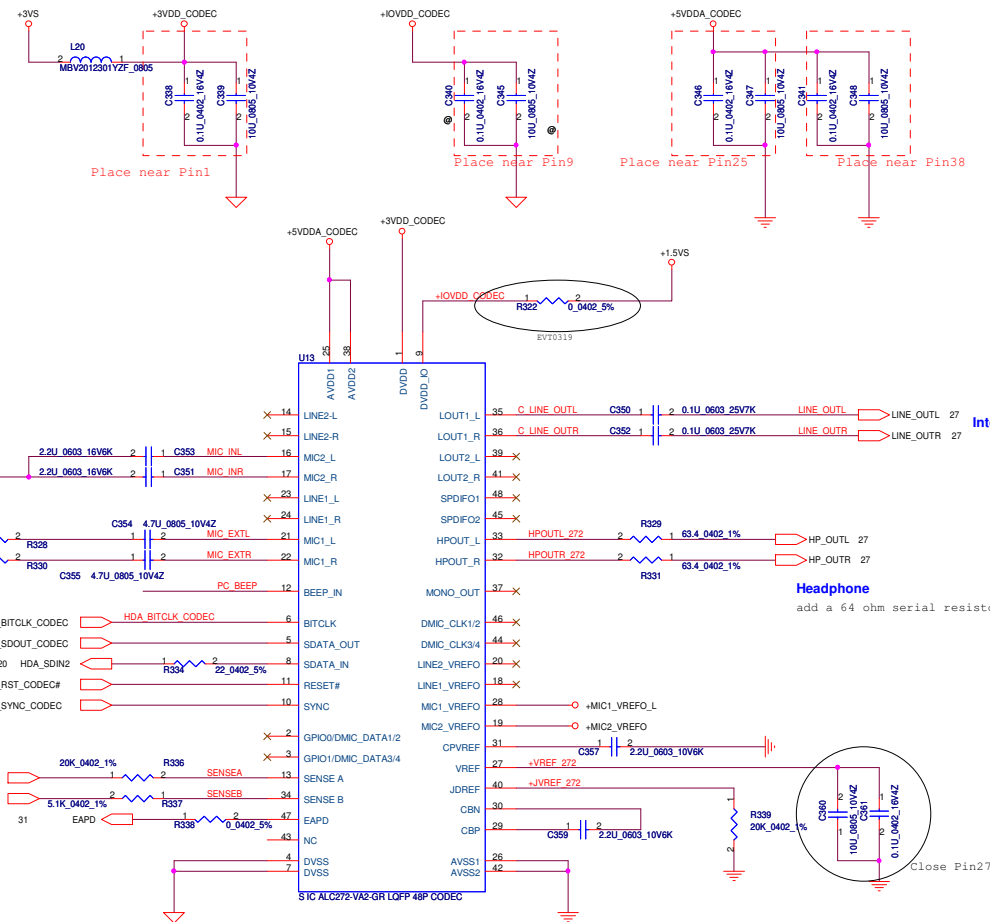
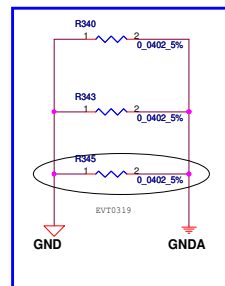
Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	NOT USE
MIC1 (Pin21/22)	External	Mic in
MONO-OUT (Pin37)	Internal	NOT USE
MIC2 (Pin16/17)	Internal	Internal Mic

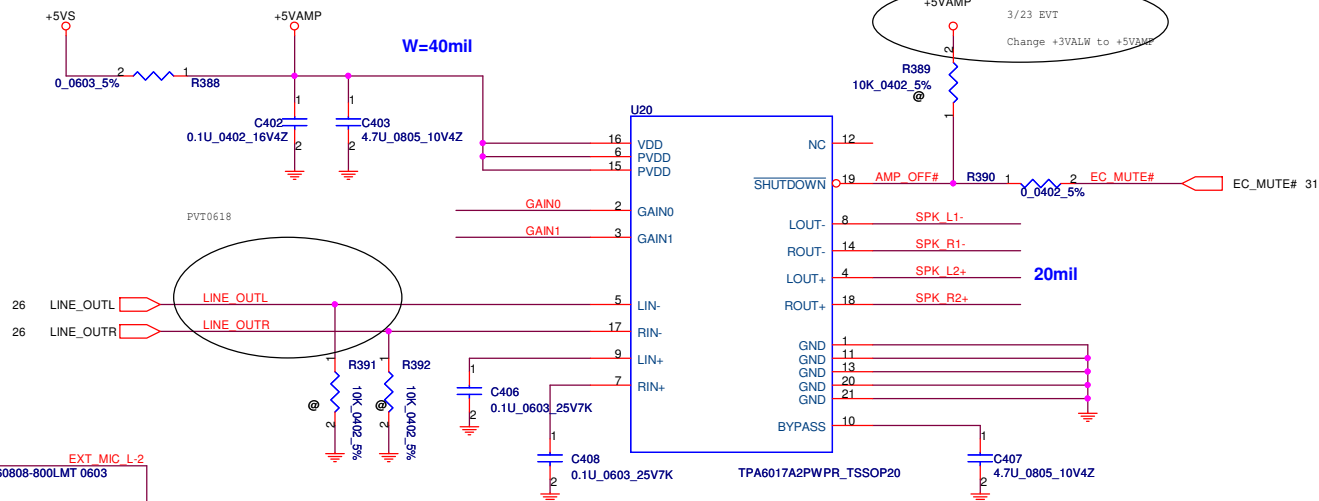
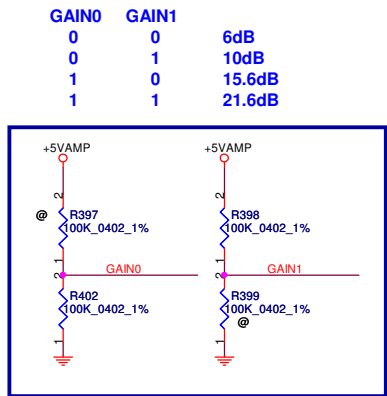


MIC Sense
R516 place near pin13
Capless HP Sense
R517 place near pin34

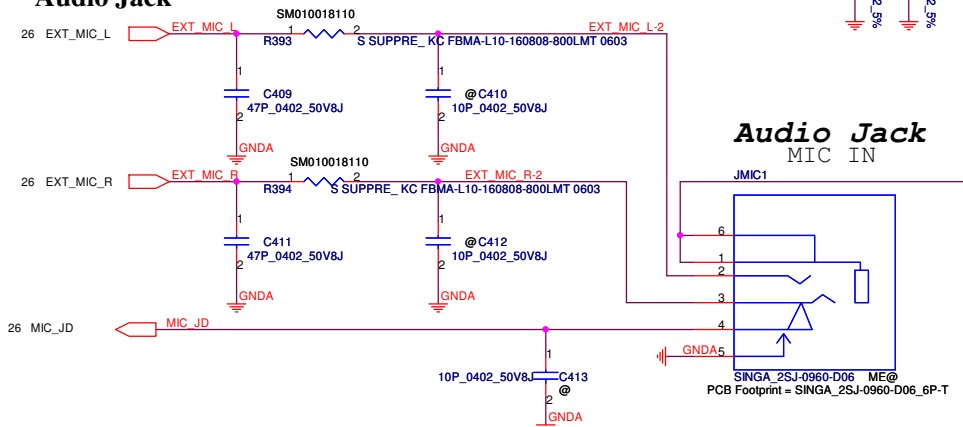
27 MIC_ID

27 PLUG_IN

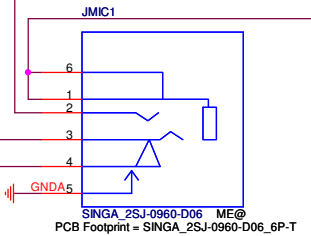




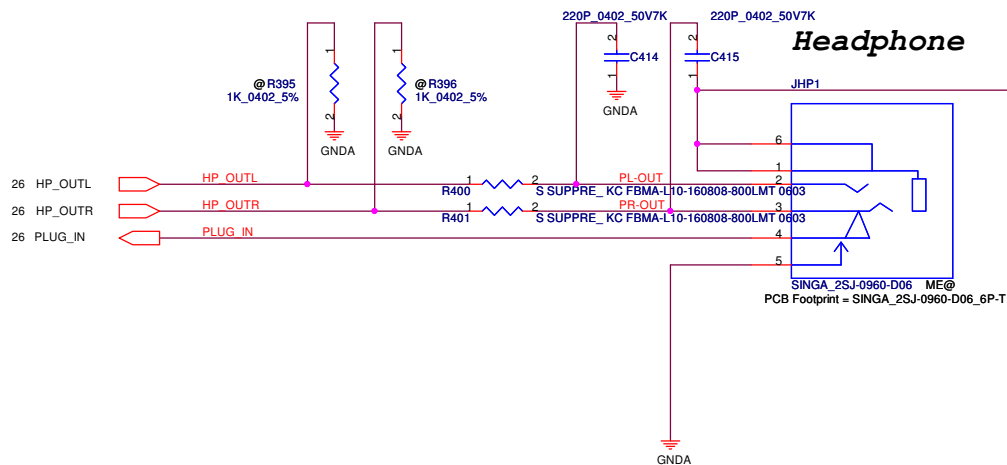
Audio Jack



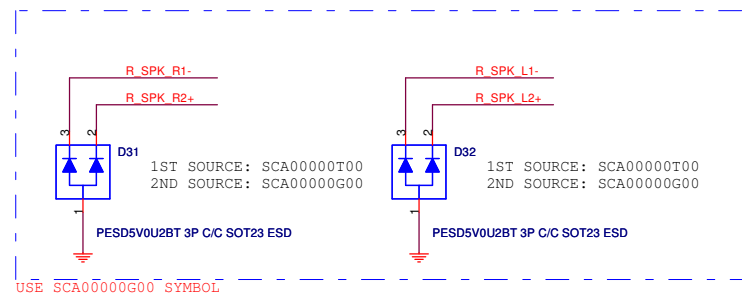
Audio Jack MIC IN



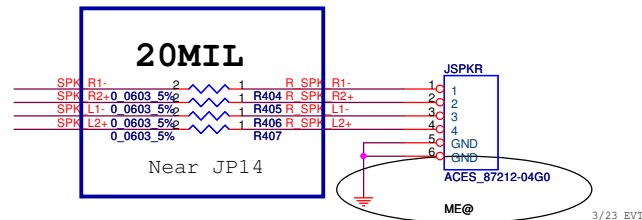
Headphone



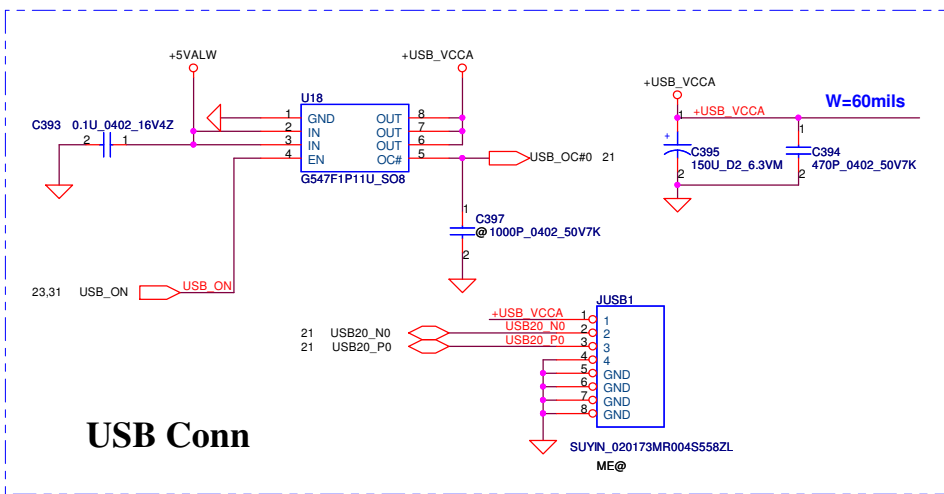
ESD PROTECT



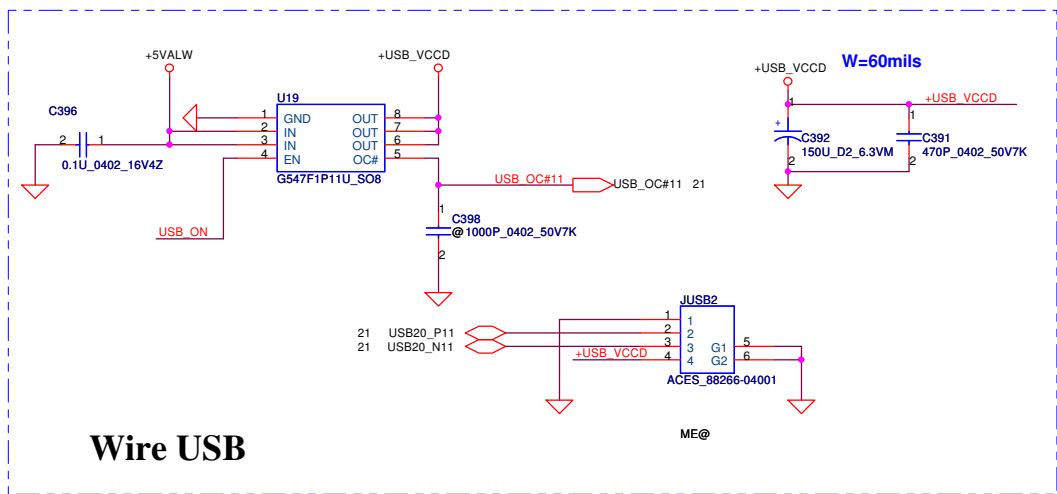
SPEAKER JACK



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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	AMP Audio speaker CONN
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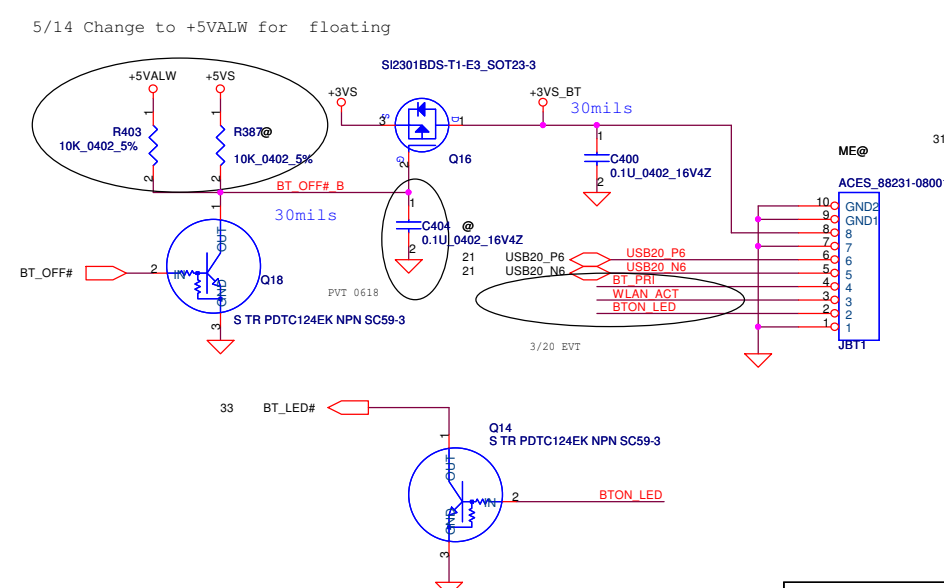
USB Conn



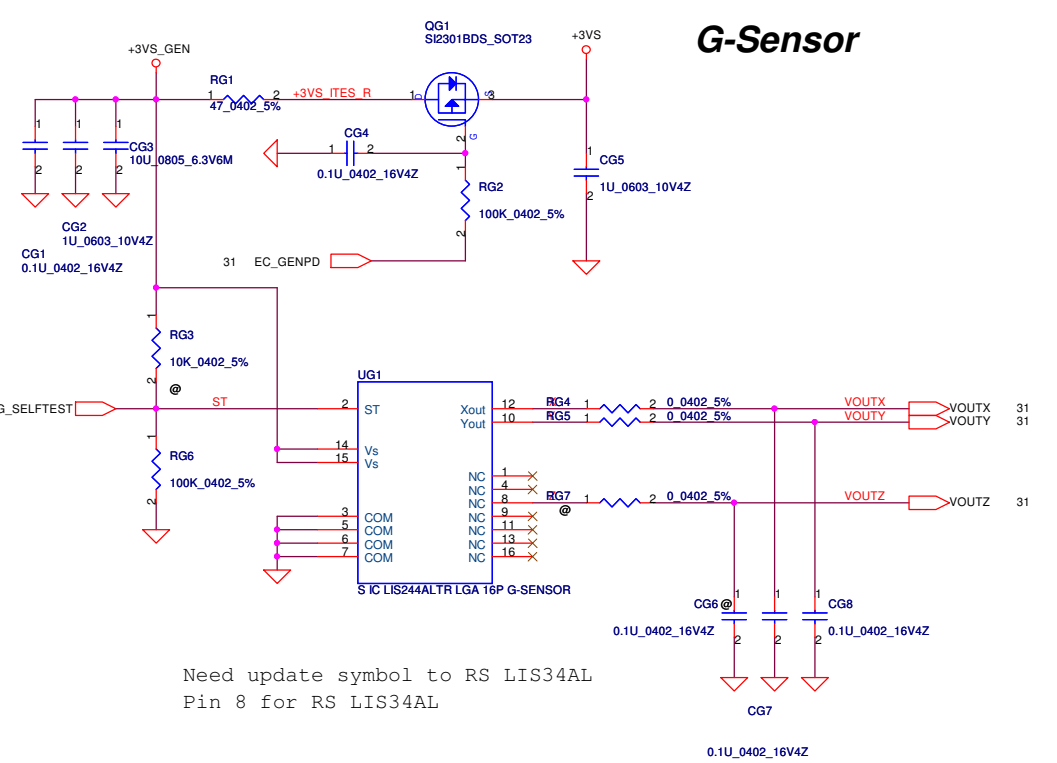
Wire USB



3/26 Remove ESD Diode ,by AndyYL



BT MODULE CONN



G-Sensor

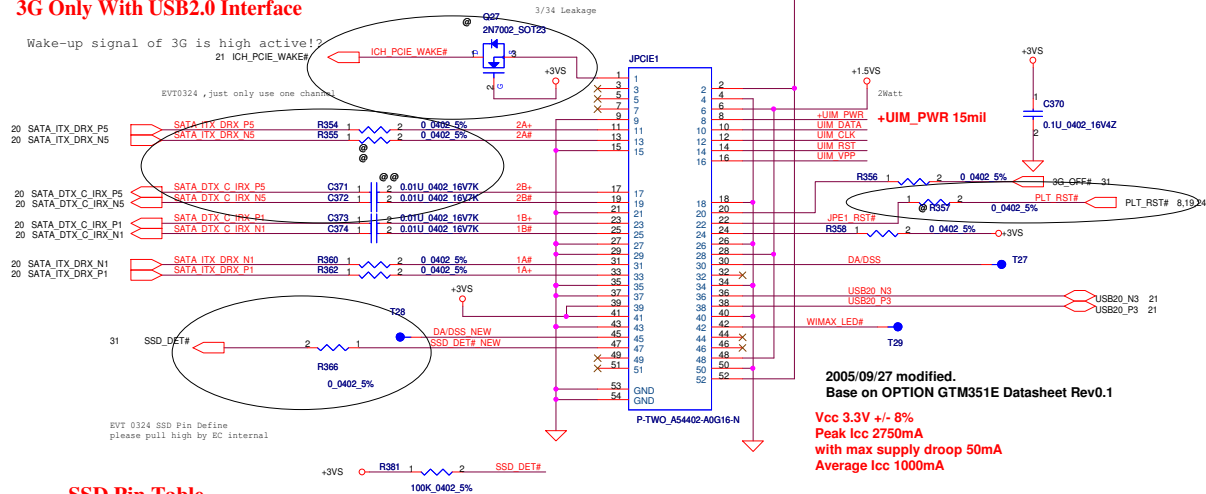
Need update symbol to RS LIS34AL
Pin 8 for RS LIS34AL

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Custom	Document Number	Rev	Date	
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WWW.AliSaler.Com

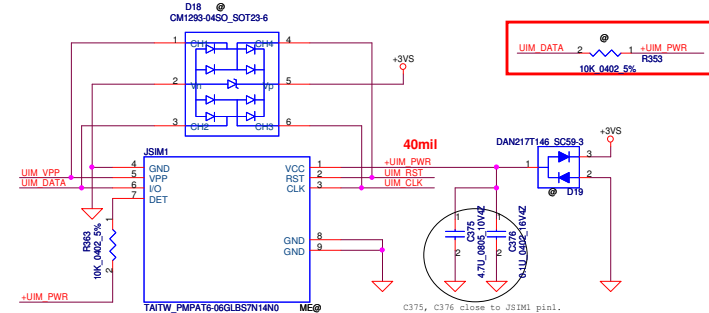
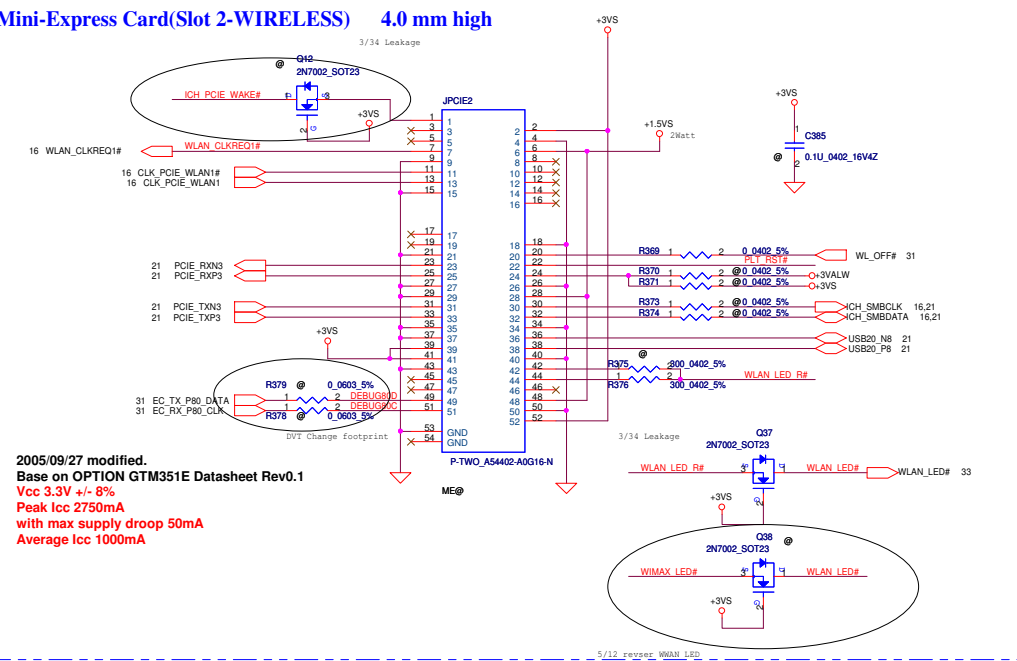
4.0 mm high

Wake-up signal of 3G is high active!

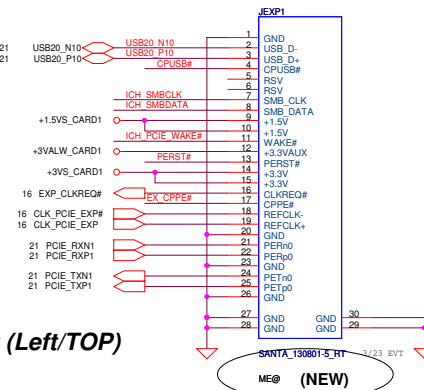


SSD Pin Table

Pin Number	SATA Assignment
11	
13	
17	
19	
23	+B (port 1)
25	-B (port 1)
30	DA/DSS
31	-A (port 1)
32	Presence Detection
33	+A (port 1)

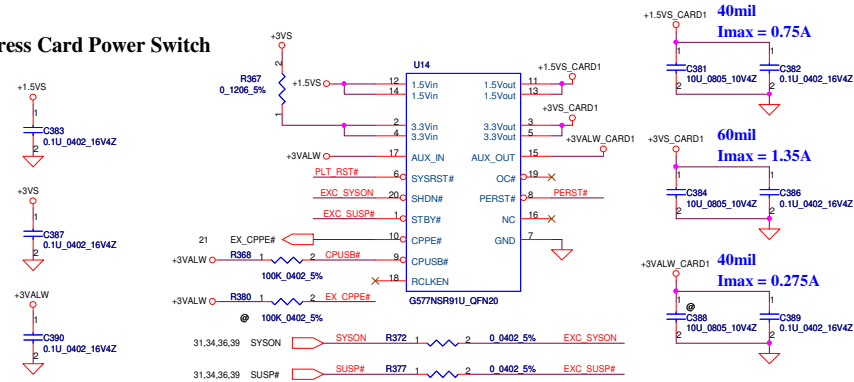


Del SIM holder backup solution.



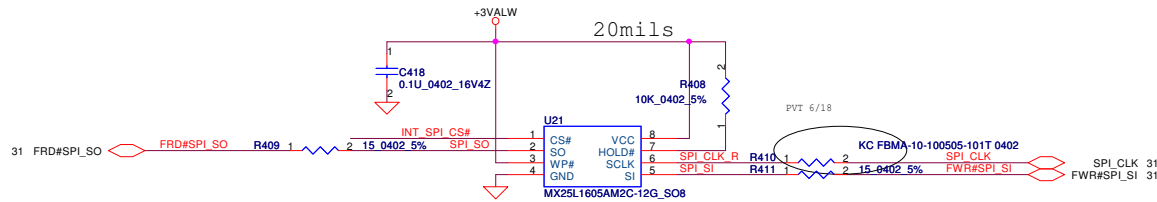
New Card 34mm Socket (Left/TOP)

Express Card Power Switch

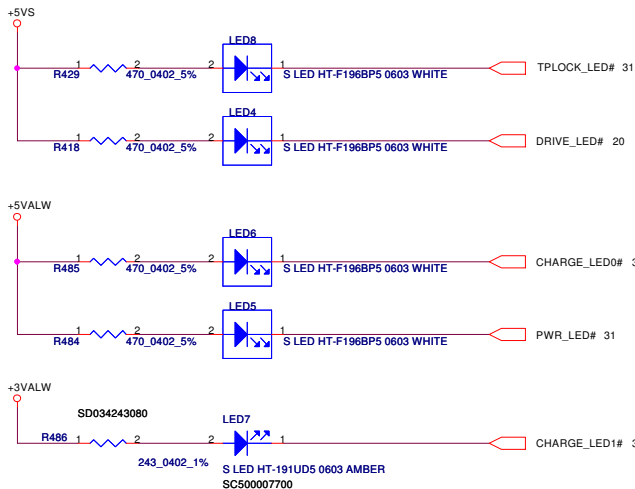
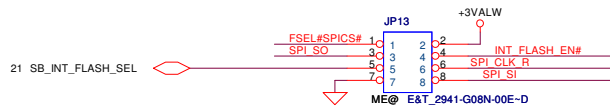
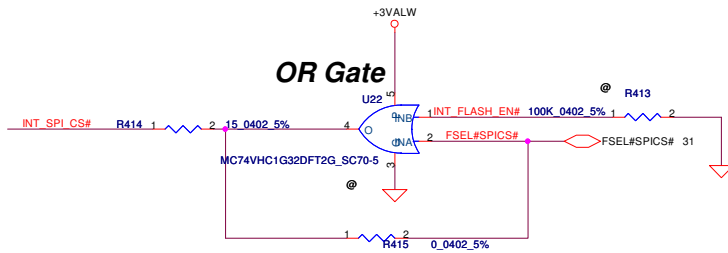


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					KIUE0_LA-5191P
Date: Thursday, June 25, 2009				Sheet	29 of 43

FOR EC 16M SPI ROM

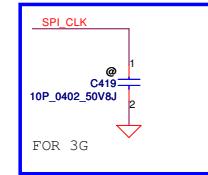
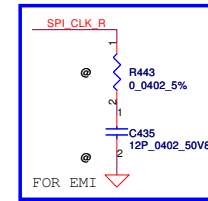


INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

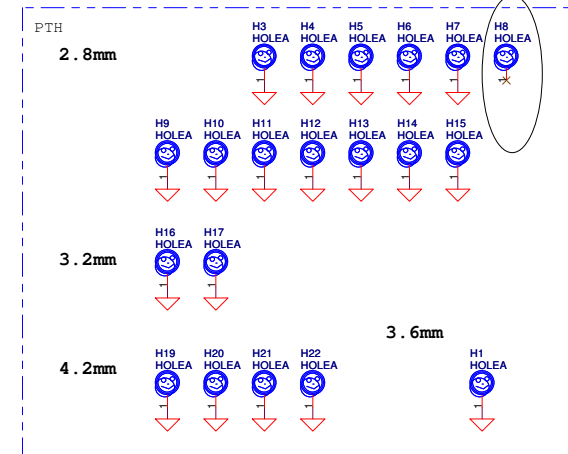
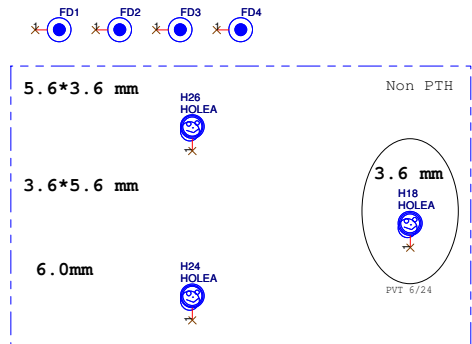


+5VLAW 470 ohm	typ	max
White LED(Vf)	2.8	3.15
current	4.6mA	3.9mA

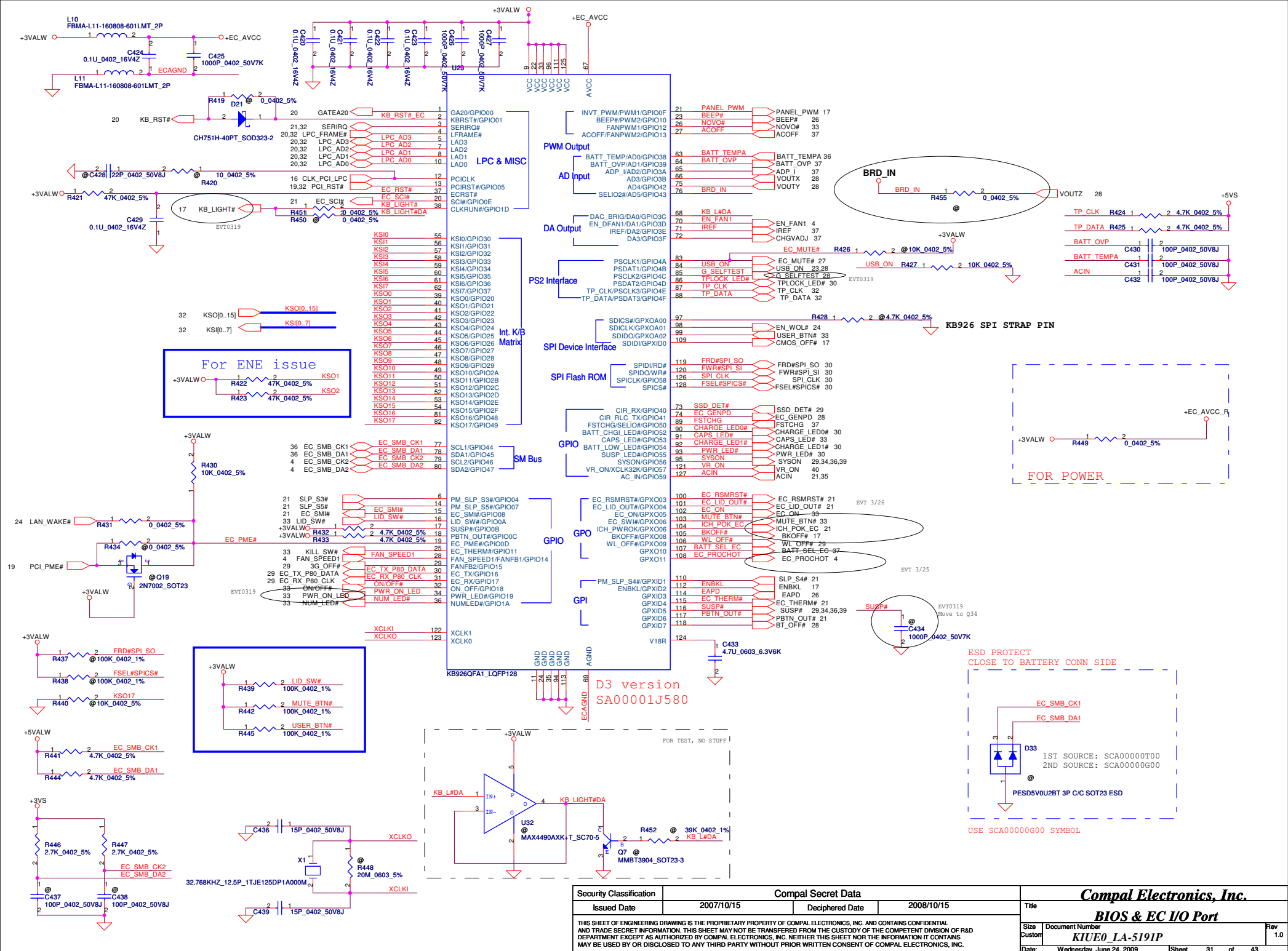
+3.3 VALW 243 ohm	typ	max
Amber LED(Vf)	1.9	2.4
current	5.7mA	3.7mA



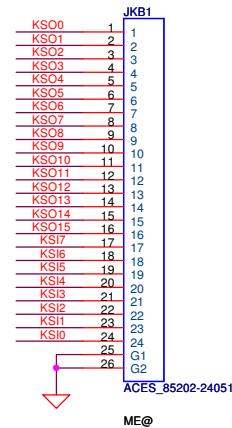
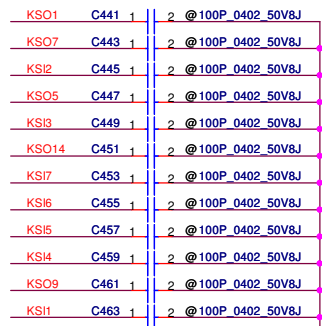
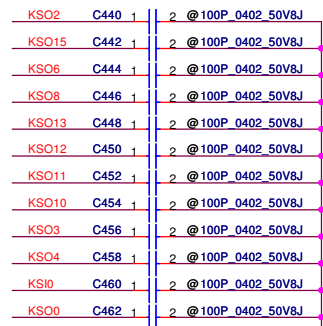
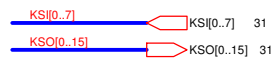
EVT 6/18 Close EC Pin



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				LED/EC SPI ROM			
Size B		Document Number			Rev 1.0		
		KIUE0_LA-5191P					
Date:		Wednesday, June 24, 2009		Sheet		30 of 43	

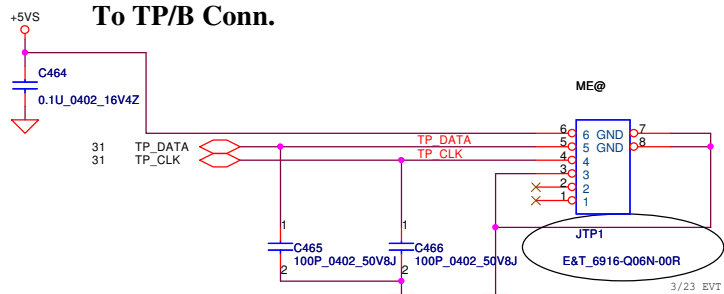


INT_KBD Conn.



CONN PIN define need double check

To TP/B Conn.

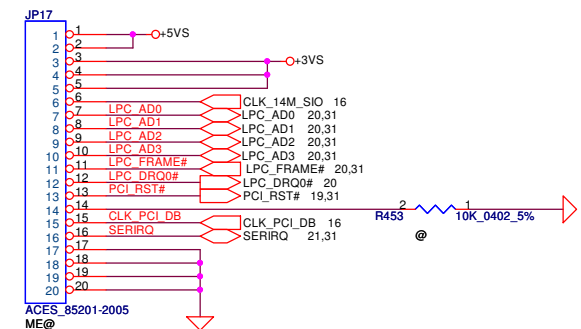


EC DEBUG PORT

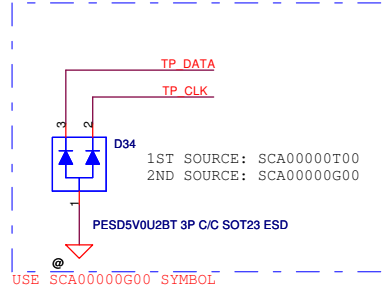
EVT0319

Delete this connector.
It same as MiniPCIE Debug Card.

FOR LPC SIO DEBUG PORT

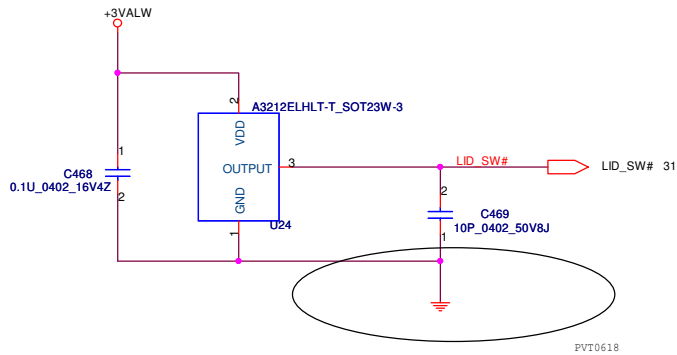


ESD PROTECT
CLOSE TO JTP1



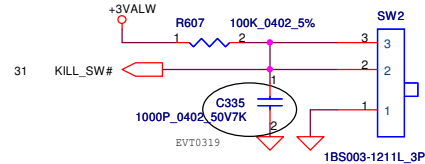
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				KB /SW /LPC Debug Conn.	
				KIUE0_LA-5191P	
				Date	Sheet
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Lid Switch



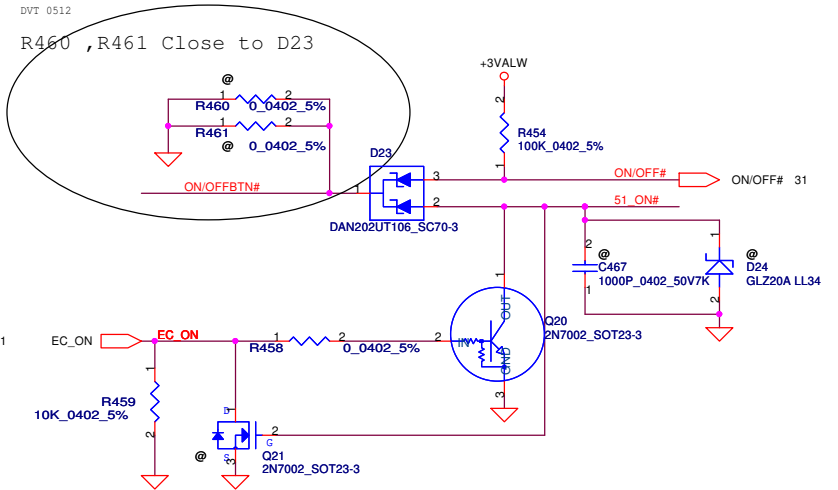
Kill Switch

EE parts.
1st: DE1000000100
2nd: DE1000000100

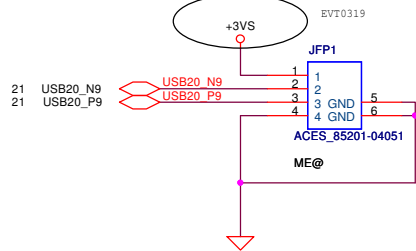


ON/OFF switch

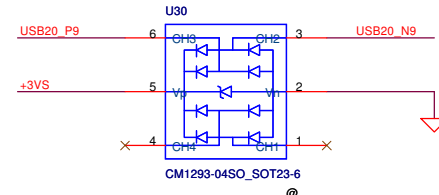
EVT0324 for debug only



FP Board Conn 4 pin

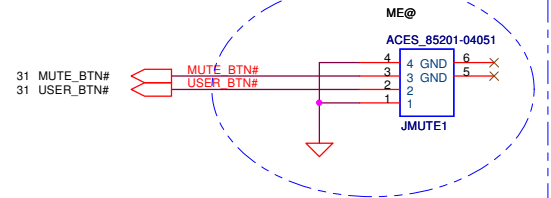


3/26 EVT
ESD PROTECT



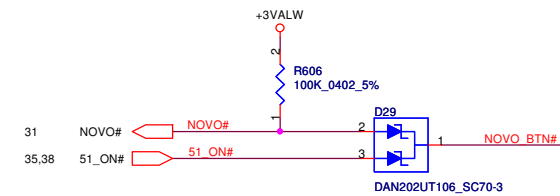
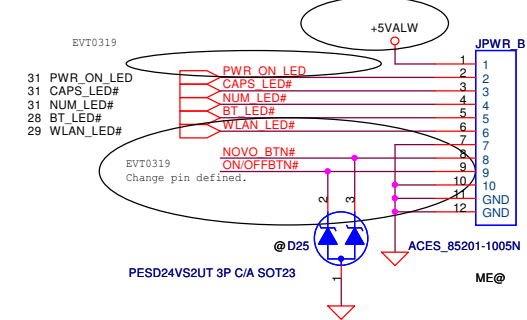
3/26 Please Close JFP1

USER SWITCH Board Conn. 4 pin



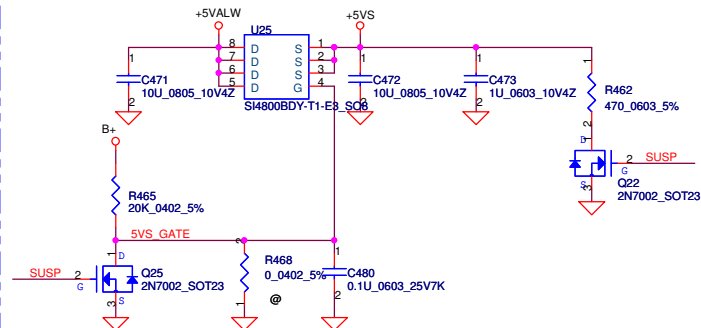
Reverse for CABLE Pin define

Power Board Conn. 10 pin

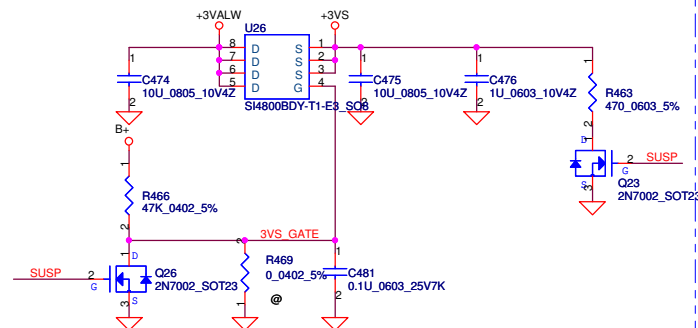


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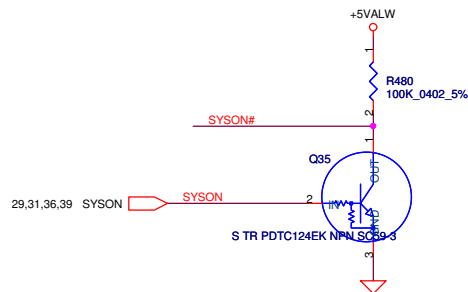
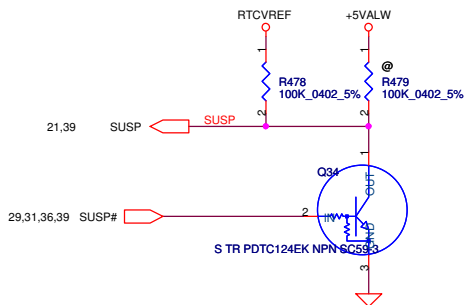
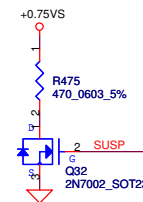
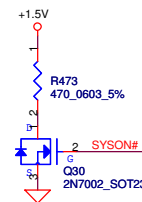
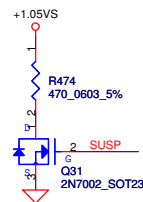
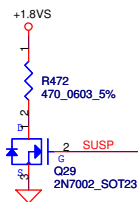
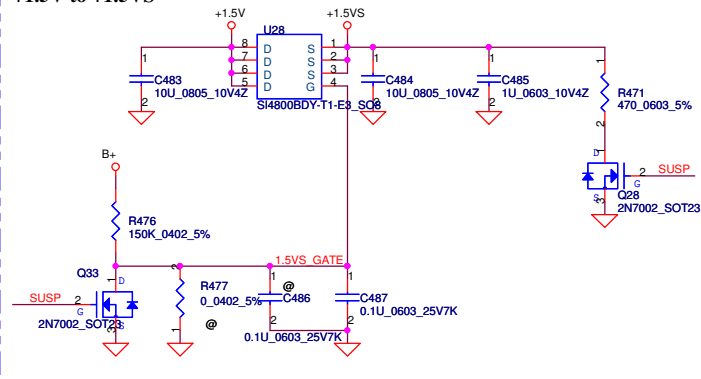
+5VALW TO +5VS



+3VALW TO +3VS

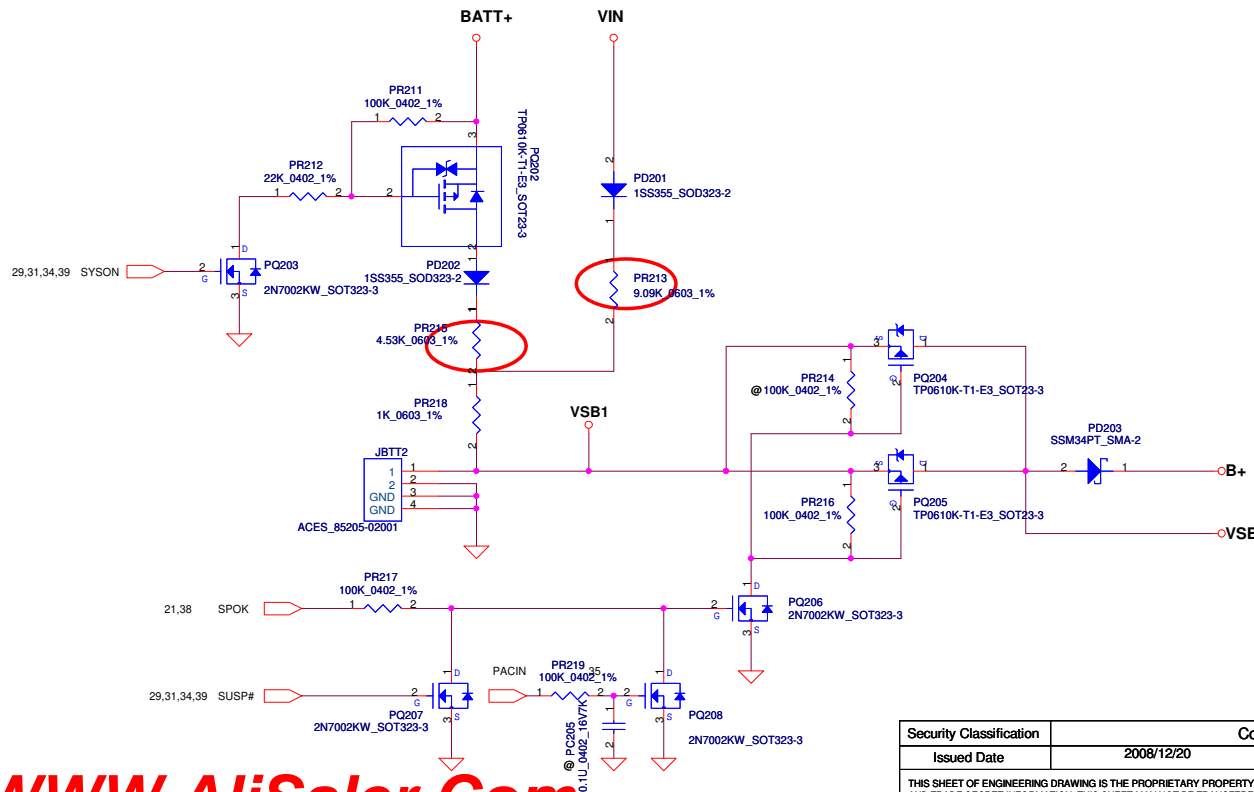
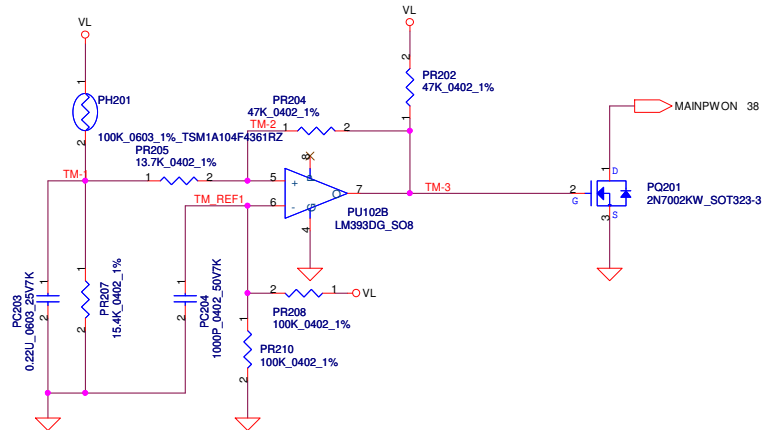
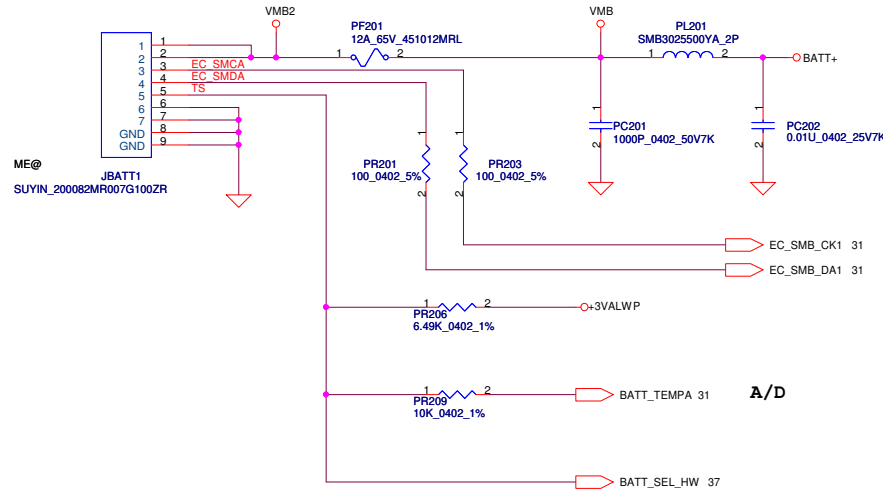


+1.5V to +1.5VS



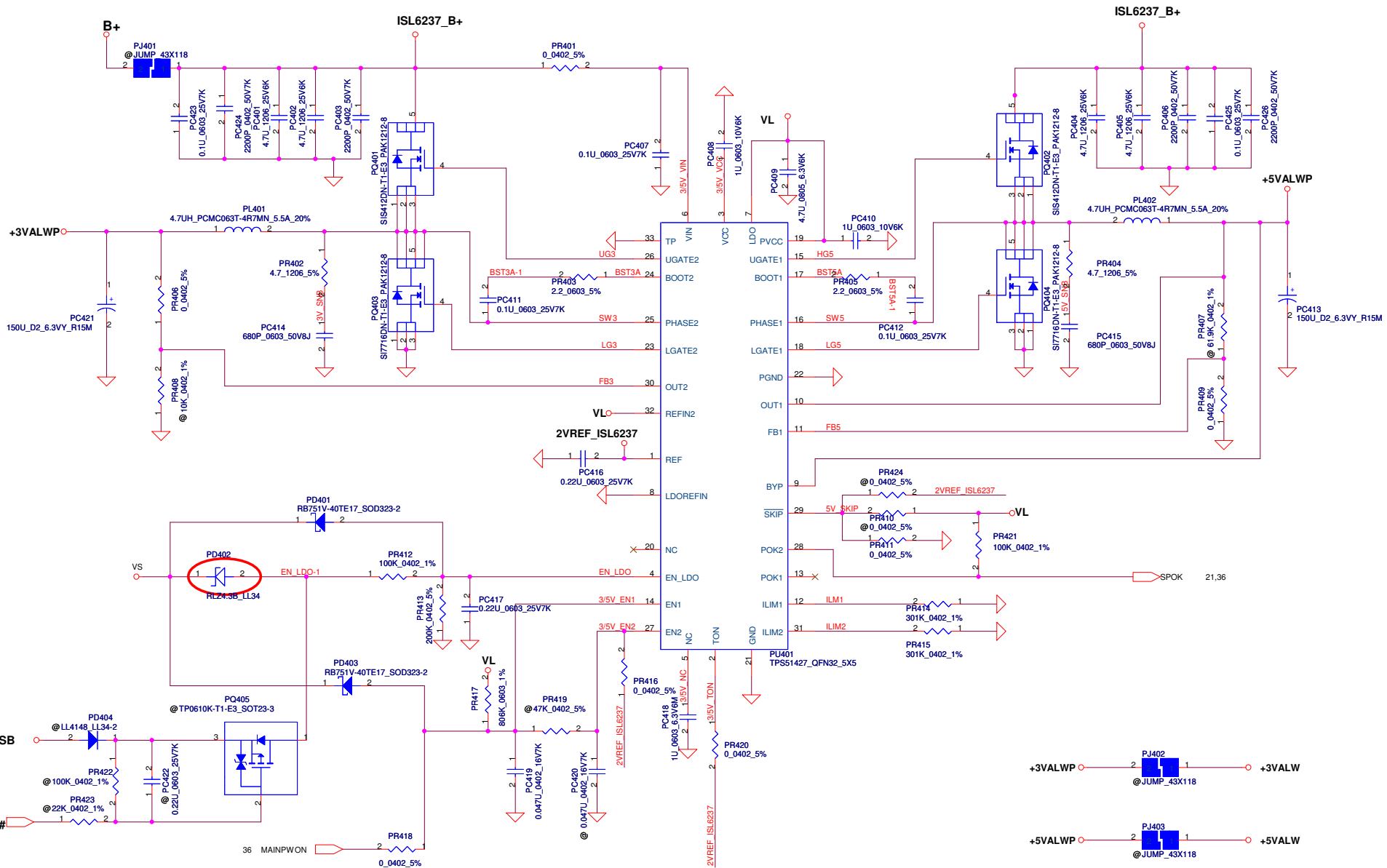
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Size	Custom	Document Number	KIUE0_LA-5191P		Rev
Date	Wednesday, June 24, 2009	Sheet	34	of	43

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

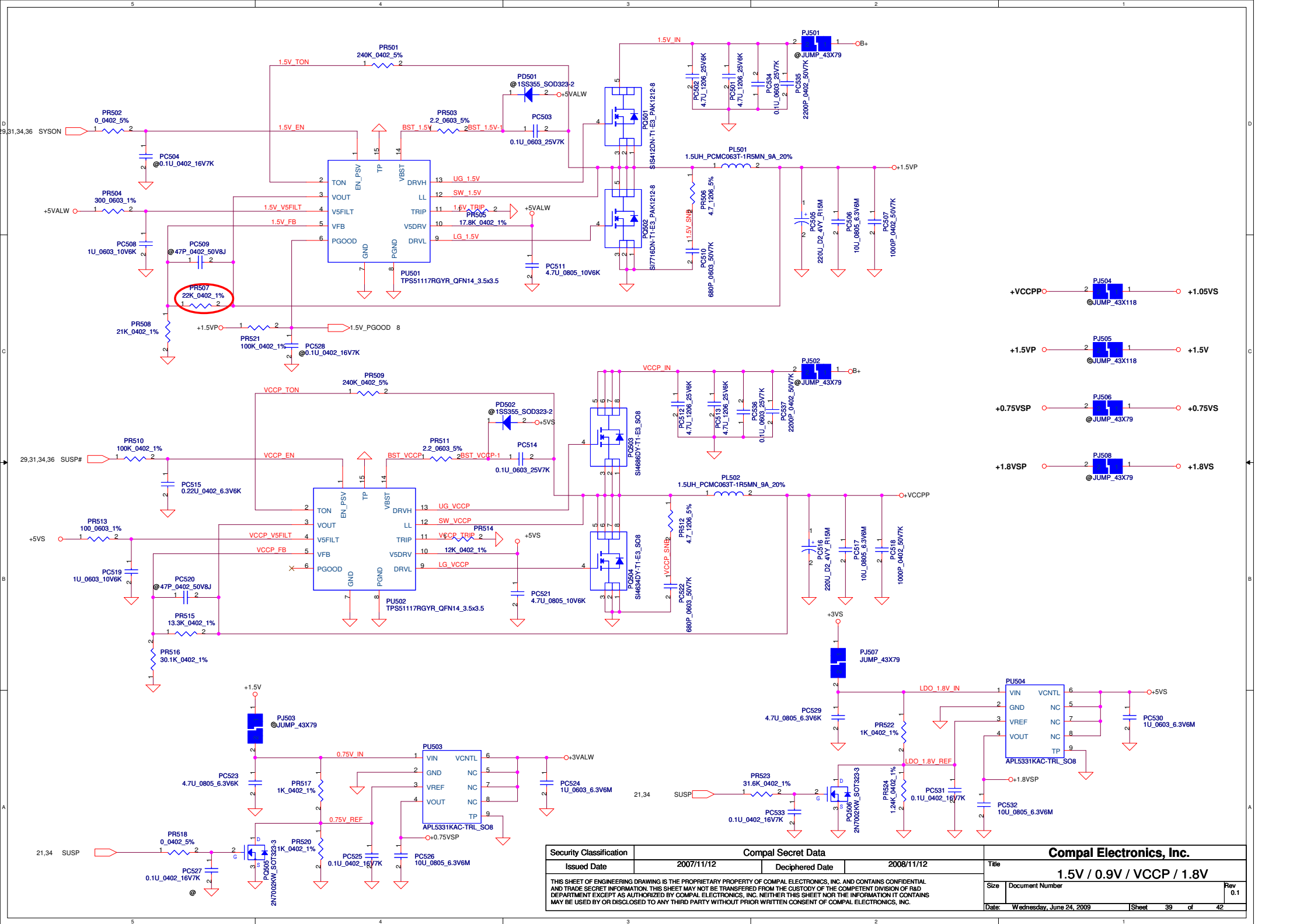


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Deciphered Date				2009/12/20				BATTERY CONN / OTP		
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Date				Wednesday, June 24, 2009				Sheet		
								36 of 42		

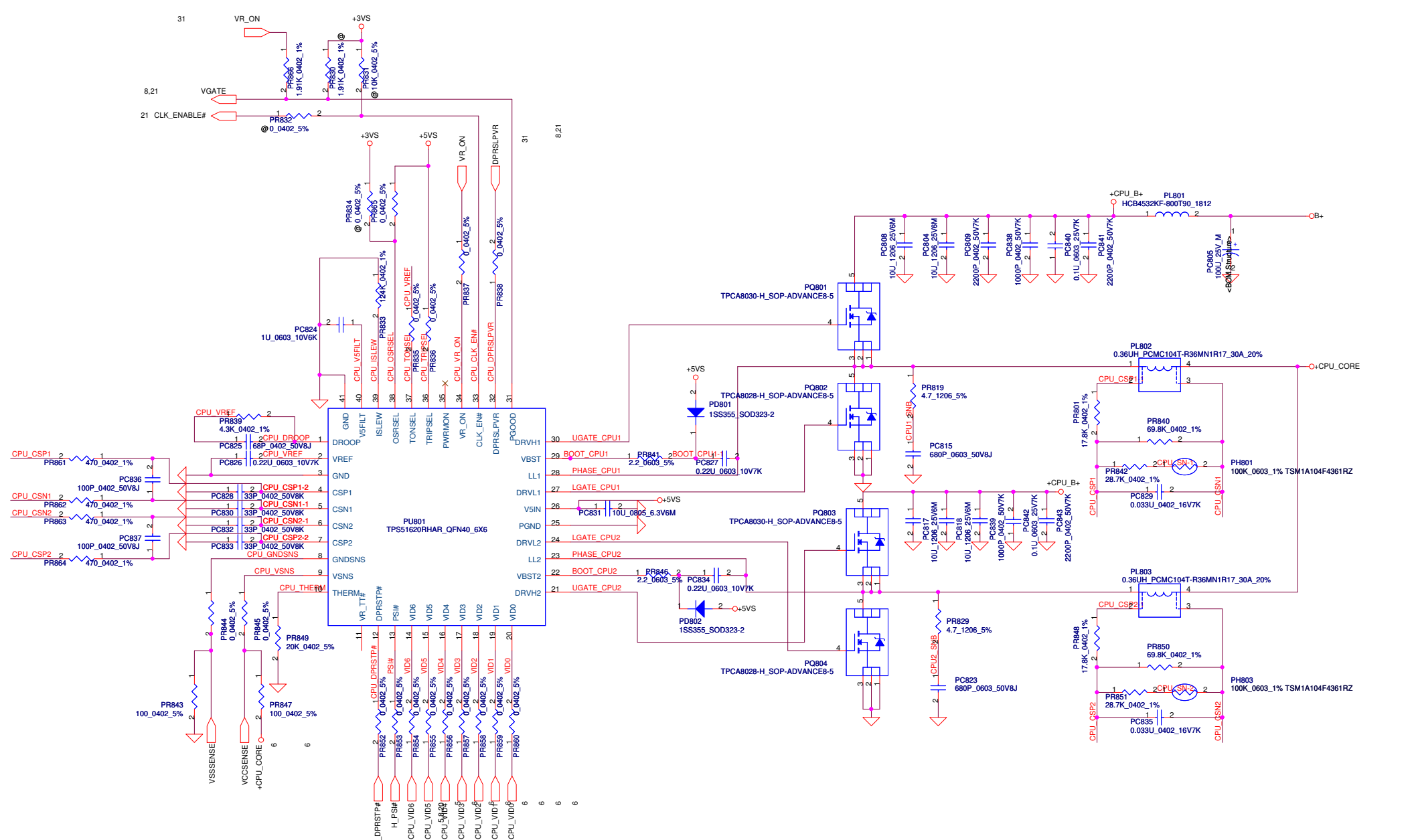
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				Date	Wednesday, June 24, 2009
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				Rev	0.1

Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change design	add bridge battery charge circuit		P.37	add PR215 and PR218 and change PR213 from 2K to 2.2K	2009.3.20	DVT
2	Change design	Change design		P.36	JDCIN turn off 180 degree	2009.3.20	DVT
3	Change design	Change design		P.37	change JBTT2 from lie to stand	2009.3.24	DVT
4	Change design	Change design		P.37	add PR219 and PC205	2009.3.25	DVT
5	Change design	Change design		P.39	change PR403 and PR405 from 0 to 2.2 ohm	2009.3.25	DVT
6	Change design	Change design		P.40	change PR503 and PR511 from 0 to 2.2 ohm	2009.3.25	DVT
7	Change design	Change design		P.41	change PR841 and PR846 from 0 to 2.2 ohm	2009.3.25	DVT
8	Change design	Change design		P.40	change PR514 from 15.4K to 12K ohm	2009.3.25	DVT
9	Change design	Change design		P.38	add PR339 PR340 PR341 and PC332	2009.5.5	PVT
10	Change design	Change design		P.41	change PR839 from 5.76K to 4.3K ohm	2009.5.15	PVT
11	Change design	Change design		P.40	change PR504 and PR513 from 422 to 300 ohm	2009.5.15	PVT
12	Change design	Change design		P.38	delect PR338	2009.6.18	Pre_MP
13	Change design	Modify bridge battery charge current		P.37	change PR213 from 2.2k to 9.09k and PR215 from 1.21k to 4.53k	2009.6.18	Pre_MP
14	Change design	Modify 1.5V output voltage		P.40	change PR507 from 21k to 22k	2009.6.18	Pre_MP
15	Change design	For bridge battery can work in S3		P.39	change PD402 from RLZ5.1B to RLZ4.3B	2009.6.18	Pre_MP
16							
17							
18							
19							
20							
21							
			Security Classification		Compal Secret Data		Compal Electronics, Inc.
			Issued Date	2007/09/20	Deciphered Date	2008/09/20	PIR (PWR)
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			Date: Wednesday, June 24, 2009				Sheet 41 of 42

25. 03/25 P.4 : Add thermal protection Circuit by lenvono
26. 03/25 P.21 : S0 to G3 state, abnormal shutdown
27. 03/25 P.21 : Change New CARD PCI-E port 4 to Port 1 for power saving
28. 03/25 P.33 : Add EMI&ESD solution
29. 03/25 P.24 : Delete Mac ROM Circuit ,Because of layout space not enough
30. 03/25 P.24 : Change Q24 to PMOS from NMOS, to saving bom cost
31. 03/25 P.26 : modify PC-BEEP circuit avoid Signal and Pwr noise

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				Custom	KIUE0_LA-5191P	1.0	
				Date:	Wednesday, June 24, 2009	Sheet 42 of 43	

Version change list (P.I.R. List)

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for EE

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Detect Bridge Battery life	Can't detect Bridge battery	0.3	31	ADD R455	5/5	DVT
2	Esay rework for PORT 80	Not easy debug with system builded	0.3	29	CHANGE R378,R379 SIZE From 0402 to 0603 (NC)	5/13	DVT
3	BT Pwer MOS Floating	BT Pwr MOS Floating	0.3	28	NC R387, ADD R403	5/13	DVT
4	WWAN Noise Solution	Reserve C470	0.3		ADD C470 (NC)	5/13	DVT
5	Material LT	LIS34ALTR LT more than 4 months	0.3	28	CHANGE UG1 From LIS34ALTR to LIS244ALTR	5/13	DVT
6	DFB Design	COST DOWN	0.3	17	DELETE R167,R168,R287,R361	5/13	DVT
7	WWLAN LED	Reverse WWAN LED SWITCH	0.3	29	ADD Q38 (NC)	5/13	DVT
8	ICH_POK Glitch	Glitch will cause abnormal Power sequence	0.3	21	ADD D35,Q39 (NC),R456 (NC)	5/13	DVT
9	EMI Solution	EMI issue	0.3	17	ADD D36	5/13	DVT
10	Soft Start circuit	OCP	0.3	24	ADD R304,C325 (NC),C122	5/13	DVT
11	Debug use only		0.3	33	DELETE J3,J4,SW1,ADD R460 (NC),R461(NC)	5/13	DVT
12	BOM Option	Reserve R121	0.3	16	CHANGE R122 From 12 Ohm to 33 Ohm	5/16	DVT
13	BOM Option	ALC272-GR EOL	0.3	20	CHANGE SA00002CI00 to SA00002CI10	5/25	DVT
14	BOM Option	DELETE ROHM MATERIAL FROM 1st BOM	0.3		CHANGE SBX01240010 to SB00000AG00	5/25	DVT
15	BOM Modify		1.0	23	CHANGE R90 SIZE From 0603 to 0805, DELETE R335,R342,R416	6/23	PVT
16	Stepping to V1.0	Update LA5191PR10 to Stepping to V1.0	1.0	01	Update DAZ P/N to V1.0 and ADD Sub-Bard P/N LS5191/LS5192/LS5193/LS5194	6/23	PVT
17	Soft START Circuit	OCP for LAN	1.0	24	Change R304 from 0 Ohm to 10K Ohm , Delete C122	6/23	PVT
18	Mic Pull high change		1.0	26	Change R333 From 4.7K Ohm to 2.2K Ohm	6/23	PVT
19	AUDIO LINE OUT CAP	Remove Duplicated Cap	1.0	27	DELETE C404,C405	6/23	PVT
20	EMI SOLUTION	SPI CLK	1.0	30	Change R410 From 15 Ohm to KC FBMA-10-100505-101T 0402	6/23	PVT
21	Soft START Circuit	OCP for Bluetooth	1.0	28	ADD C404 (NC)	6/23	PVT
21	Soft START Circuit	OCP for CAMERA	1.0	17	ADD C416 (NC)	6/23	PVT

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